Study for Mechanical Stress Impact in Scaled MOSFETs

Nuo Xu, Lynn Wang, Xin Sun, Prof. Andrew Neureuther, Prof. Tsu-Jae King Liu

Electrical Engineering and Computer Sciences Department
University of California at Berkeley
Introduction

• Uniaxial Stress Technology is already in production since…

Intel 90nm HP Tech.


Intel 45nm LP Tech.


• MOSFET Performance is Largely Improved

D. Chanem et al, 2005 Symp. VLSI Tech.


• Systematic Transistor Variations

<table>
<thead>
<tr>
<th>Layout</th>
<th>90nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/D Stress</td>
<td>NA</td>
<td>$\Delta F \sim 5%$</td>
</tr>
<tr>
<td>STI</td>
<td>NA</td>
<td>$\Delta F \sim 3%$</td>
</tr>
<tr>
<td>Etch</td>
<td>$\Delta F &gt; 10%$</td>
<td>$\Delta F \sim 2%$</td>
</tr>
<tr>
<td>Litho</td>
<td>$\Delta F \sim 1%$</td>
<td>$\Delta F \sim 1%$</td>
</tr>
</tbody>
</table>

*L.-T. Pang et al., 2006 Symp. VLSI Circuits*
Outline

• Introduction
• Fast-models for Stress-induced Variations
• Injection Velocity Model for Strained MOSFET
• 3D Stress Design for Multigate FET
Stress-Layout Dependence

- The Impact of Process-induced Stress Variations on MOSFET:

  - **SPICE/Compact models**: Adjust mobility and threshold voltage empirically by fitting a few layout parameters:
    - Models are too simplistic, do not capture all layout parameter effects
  
  - **TCAD simulations**: numerical (FEM) analysis to determine full stress profiles in the transistor
    - Computationally expensive

→ Need a fast, accurate method for determining channel stress profile, for accurate estimation of transistor performance
Flamant Solution

- Analytical solution to concentrated force problems in an infinite large plane

Classical:

\[
\begin{align*}
\sigma_r &= \frac{1}{r} \left[ (a_{12} + 2b_{15}) \cos \theta + (b_{12} - 2a_{15}) \sin \theta \right] \\
\sigma_\theta &= \frac{1}{r} \left[ a_{12} \cos \theta + b_{12} \sin \theta \right] \\
\tau_{r\theta} &= \frac{1}{r} \left[ a_{12} \sin \theta - b_{12} \cos \theta \right]
\end{align*}
\]

Actual:

Stress contours \( \sigma_x \) and \( \sigma_y \) distributions

Graph showing stress contours and stress \( \sigma_x \) and \( \sigma_y \) distributions:

- Graph with axes labeled: x, y, and stress \( \sigma_x \) and \( \sigma_y \)
- Legend indicating numerical TCAD and analytical model

Table with physical parameters:

- Lg = 40nm
- Tox = 1nm
- spacing (to channel centre): 90nm
- Initial stress: Tensile 2GPa
- Stressor thickness: 60nm
- Stressor area: 2nm x 2nm

Graph showing stress vs. distance from channel centre:

- Axes: Distance from channel centre (um) vs. Stress XX (Pa)
- Trends for numerical TCAD and analytical model

Graph showing stress contours:

- Active Channel
- Point Source
- Gate Edge
- Graph with axes labeled: Distance from channel centre (um) vs. Stress XX (Pa)
Simulation Approach

1. Perform 3-D TCAD simulations to determine the channel stress profiles ($\sigma_{XX}$, $\sigma_{YY}$) induced by a point source in the source/drain region
2. Fit analytical models to the simulated stress profiles
3. Integrate point-source contributions to obtain the full channel stress profiles
**Point-source Stress Function**

\[
S_1 = \frac{S_{xx,0}}{r^\alpha \sin^3 \theta} \\
S_2 = S'_{xx} \left( \frac{1}{r_1^\beta e^{L_0^x}} + \frac{1}{r_2^\beta e^{L_0^x}} \right)
\]

**Stress XX**

F.S. Term: \( S_1 = \frac{S_{yy,0}}{r^\alpha \cos^3 \theta} \) - 0.02 - 0.01 0.00 0.01 0.02

Correc. Term: \( S_2 = S_{yy}' \left( \frac{r_1}{r_0} e^{\frac{x}{L_0}} \right) \) (right side)

Correc. Term: \( S_2 = S_{yy}' \left( \frac{r_2}{r_0} e^{-\frac{x}{L_0}} \right) \) (left side)

**Stress YY**

F.S. Term: \( S_1 = \frac{S_{yy,0}}{r^\alpha \cos^3 \theta} \) - 0.02 - 0.01 0.00 0.01 0.02

Correc. Term: \( S_2 = S_{yy}' \left( \frac{r_1}{r_0} e^{\frac{x}{L_0}} \right) \) (right side)

Correc. Term: \( S_2 = S_{yy}' \left( \frac{r_2}{r_0} e^{-\frac{x}{L_0}} \right) \) (left side)
Channel Stress Profiles

Impact from STI

Stress YY
Stress Values (Pa)
Position along Channel Width (um)
STIV = 0nm
STIV = 50nm
STIV = 100nm
STIV = 200nm

Stress XX

Model
STIP=100nm, STIV=100nm
STIP=50nm, STIV=100nm
STIP=100nm, STIV=50nm

LOD = 0.5um; W = 0.3um; Lg = 40nm
STIP = 0.1um; STIV = 0.1um
CESL 2GPa Tensile
Model Verification with TCAD-1

- LOD Impact

\[ \text{Stress XX (Pa)} \]
\[ \text{Position along Channel Length (um)} \]
\[ \text{LOD = 700nm} \]
\[ \text{LOD = 500nm} \]
\[ \text{LOD = 300nm} \]
\[ \text{Model} \]

\[ \text{Stress YY (Pa)} \]
\[ \text{Position along Channel Width (um)} \]
\[ \text{LOD = 700nm} \]
\[ \text{LOD = 500nm} \]
\[ \text{LOD = 300nm} \]
\[ \text{Model} \]
Model Verification with TCAD-2

- **Channel Width Impact**
Verification with Silicon Data

Intrinsic Transistor Delay
\[ \tau = \frac{V_{dd} - V_{th} + \frac{C_i V_{dd}}{C_{inv} L_g} l_g}{(3 - \delta) \frac{V_{dd}}{4} - V_{th} v_{inj}} \]

Mobility %
\[ \frac{\Delta \mu}{\mu} = - (\Pi_{xx} S_{xx} + \Pi_{yy} S_{yy}) \]

Injection Velocity %
\[ \frac{\Delta v_{inj}}{v_{inj}} = \left[ \alpha + (1 - B)(1 - \alpha + \beta) \right] \frac{\Delta \mu}{\mu} \]

Threshold Voltage %
\[ \Delta V_{th} = (m - 1) \left[ \Delta E_g + \frac{kT}{q} \ln \left( \frac{N_v(0)}{N_v(S_{eff})} \right) \right] \]

Effective Current %
\[ \frac{\Delta I_{eff}}{I_{eff}} = \frac{\Delta v_{inj}}{v_{inj}} - \frac{\Delta V_{th}}{(3 - \delta) \frac{V_{dd}}{4} - V_{th}} \]

RO Frequency %
\[ \frac{\Delta f_{RO}}{f_{RO}} = \frac{\Delta I_{eff}}{I_{eff}} + \frac{\Delta V_{th}}{V_{dd} - V_{th} + \frac{C_i V_{dd}}{C_{inv} L_g}} \]

Test Chip information:
E. Josse et al, IEDM (2006)
Predictive Device Modeling

What limits the ON-state current for modern transistors?

Drift + Diffusion

Quasi-Ballistic

\[ L_g \gg \lambda \]

\[ L_g \sim \lambda \text{ (20nm for Si)} \]

High-field Saturation Velocity (Drain side)

\[ I_D = W C_{ox} \nu_{sat} (V_{GS} - V_T) \]

Low-field Mobility (Along whole channel)

Injection Velocity (Source edge)
Compact Modeling Flow

Injection Velocity Model


\[ I = \frac{qW \sqrt{2m_y} \left( \frac{k_B T}{\pi} \right)^{\frac{3}{2}}}{2 \hbar^2} (1 - R) \left[ \mathfrak{J}_{\frac{1}{2}}(E_{f1}) - \mathfrak{J}_{\frac{1}{2}}(E_{f2}) \right] \]

Critical Length
\[ l = L_g \times \sqrt{\frac{k_B T}{qV_d}} \times \tan^{-1} \left( \sqrt{\frac{qV_d}{k_B T}} \right) \]

Backscattering Rates
\[ R = \frac{l}{l + \lambda_0} \]

Mean Free Path
\[ \lambda = \left( \frac{2\mu k_B T}{\nu T} \right) \frac{\mathfrak{J}_{\frac{3}{2}}(E_f)}{\mathfrak{J}_{\frac{1}{2}}(E_f) \times \mathfrak{J}_{\frac{1}{2}}(E_{f1})} \]
Model Verification

Experiment data from:

- Only 4 fitting parameters
- Physically-based, Predictive
Model Prediction

Technology Parameters from ITRS 2007

<table>
<thead>
<tr>
<th>HP Tech Node</th>
<th>90nm</th>
<th>68nm</th>
<th>52nm</th>
<th>40nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$ (nm)</td>
<td>32</td>
<td>25</td>
<td>20</td>
<td>16</td>
</tr>
<tr>
<td>$T_{inv}$ (nm)</td>
<td>1.93</td>
<td>1.84</td>
<td>1.04</td>
<td>0.82</td>
</tr>
<tr>
<td>Body Doping ($\text{cm}^{-3}$)</td>
<td>3.3e18</td>
<td>4.8e18</td>
<td>4.1e18</td>
<td>6.6e18</td>
</tr>
<tr>
<td>S/D Series Resistance (Ohm.,um)</td>
<td>180</td>
<td>200</td>
<td>200</td>
<td>180</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>1.1</td>
<td>1.1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

$\tau = \frac{V_{dd} - V_{th} + \frac{C_f V_{dd}}{C_{inv} L_g} L_g}{(3 - \delta) \frac{V_{dd}}{4} - V_{th} v_{\text{inj}}}$

- Stress benefits decrease as $L_g$ scales
- Modern bulk MOSFETs are still far from ballistic limits
Planar & 3D MOSFET Design

MuGFET Design Rule

Performance Benefits

Reduced Variations

*J.G. Fossum, IEDM 2004

*X. Sun, EDL 29,p493(2008)

*X. Sun, to be published
3D Stress Design for MuGFETs

- Various Stress Configurations

a) Uniaxial Stress (CESL)
- $S_{xx} : S_{zz} = 1 : -1$
- NMOS: Tensile
- PMOS: Compressive

b) Biaxial Stress
- $S_{xx} : S_{yy} = 1 : 1$
- NMOS: Tensile
- PMOS: Tensile & Compressive

c) Transverse Stress (Metal Gate)
- $S_{yy} : S_{zz} = 1 : 1$
- Only transverse direction
- Compressive
• Experiments

- Split-CV for mobility extraction [110]&[100] Fin
- Biaxial Tensile bending stress was applied: 0.11% ~ 200MPa
- Strained Metal Gate Devices
• Simulation (Fully Quantum Mechanical)

N-MuGFET
- 2D Poisson-EMA Schrodinger
- Analytical model for strain impact
- Non-parabolic E-k for mobility calculation

P-MuGFET
- 2D Poisson-6x6 K.P
- Luttiger-Kohn Hamiltonian, with strain impact coupled
- Detailed E-k for mobility calculation

Parameter set (calibrated with experiments):

**NMOS:**
- $D_{ac} = 14.7\text{ eV}$
- $D_{k_{LO}} = 11 \times 10^{10} \text{ eV/m}$  \( hw_{LO} = 64\text{ meV} \)
- $D_{k_{TO}} = 2 \times 10^{10} \text{ eV/m}$  \( hw_{TO} = 64\text{ meV} \)
- $D_{k_{TA}} = 2 \times 10^{10} \text{ eV/m}$  \( hw_{TA} = 48\text{ meV} \)

**PMOS:**
- $D_{ac} = 9.6\text{ eV}$
- $D_{k} = 12.9 \times 10^{10} \text{ eV/m}$
- $hw = 61.2\text{ meV}$

**Surface Roughness:**
- (100) Top surface: $\Delta = 3.30\text{A}$, $\Lambda = 20\text{A}$
- (100) Sidewall: $\Delta = 4.05\text{A}$, $\Lambda = 20\text{A}$
- (110) Sidewall: $\Delta = 6.90\text{A}$, $\Lambda = 26\text{A}$
MuGFET Universal Mobility

- Simulation & Measurements

**Electron**

![Electron Mobility Graph](image)

**Hole**

![Hole Mobility Graph](image)

Electron Mobility (cm²/V·s) vs. Inversion Density (cm⁻²). Simulation results are shown in red, while different material orientations and gate configurations are represented by various markers and colors. The graphs illustrate the mobility variation under different conditions and highlight the benefits of using MuGFET technology in various applications.
Mobility vs. Different Types of Stress

- Simulation Results

Electrons

- <110> CESL
- <110> Bi. Tens.
- <110> Gate

Holes

- <100> CESL
- <100> Bi. Comp.
- <100> Gate

- <110> channel/fin is more sensitive to stress
- CESL stress gives largest mobility enhancement
Bench Marking between FinFET & TriGate

• Simulation Results

Electrons

Holes

FinFET-like: TriGate:

$T_{Si} = 1/3 \, Lg$

$T_{Si} = Lg$

$H_{Si} = Lg$

$H_{Si} = 1/3 \, Lg$
MuGFET Injection Velocity

- Simulation Results

Electrons

- <110> channel/fin has large stress enhancement
- TriGate & FinFET is similar due to effective mass domination
- Simulation compared with published planar CMOS measured data

Holes

- V_{ds} = 1 V
- N_{inv} = 1 \times 10^{13} \text{ cm}^{-2}

- V_{ds} = -1 V
- N_{inv} = 1 \times 10^{13} \text{ cm}^{-2}
Summary

• A Fast Way to evaluate stress-induced layout dependent variations
  ➢ physically-based functions, rely on few parameters
  ➢ very fast, yet accurate enough for DFM research
• A Compact Model for MOSFET I-V under quasi-ballistic regime
  ➢ Only 4 fitting parameters
  ➢ Predictive for future technology node transistor performance
• A Quantum Simulation Approach for MuGFET mobility study
  ➢ Design the stress strategy for 3D MOSFET structures
  ➢ Explore new physical phenomena for scaled devices
• … …

Stress will be used … to the end of CMOS!
New problems research opportunities raised for scaled devices
Acknowledgements

• IMPACT program & UC Discovery Grant
• UC Berkeley Graduate Fellowship
• Test chips donated from STMicroelectronics & Texas Instruments