MOSFET Carrier Velocity in the Quasi-Ballistic Regime: Insights for Nanoscale MOSFET Design

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Outline

• Introduction

• Predictive Modeling of Strained Nano-scale MOSFETs

• Study of Carrier Transport in Multi-Gate FETs

• Summary
MOSFET Scaling Challenges

- Improvements in IC performance and cost have been enabled by the steady miniaturization of the transistor:
  - Transistor Scaling
  - Investment
  - Better Performance/Cost
  - Market Growth

- Power density now limits transistor scaling.
  - Advanced materials and structures that improve performance and/or reduce variability are needed to facilitate voltage ($V_{DD}$) scaling.

Source: B. Meyerson (IBM)
Semico Conf., January 2004
MOSFET Basics

• Current flowing between the Source and Drain is controlled by the voltage applied to the Gate.

• The greater the capacitive coupling between the Gate and the channel, the better control the gate has over the channel potential.

  ✓ higher $I_{ON}/I_{OFF}$ for a given $V_{DD}$, or lower $V_{DD}$ to achieve target $I_{ON}/I_{OFF}$
  ✓ reduced short-channel effect (SCE) & drain-induced barrier lowering (DIBL)
    $\rightarrow$ less $V_T$ variation due to random dopant fluctuations (RDF), gate line-edge-roughness (LER)

Electron Energy Band Profile

$n(E) \propto \exp(-E/kT)$
Performance Boosters

- High-permittivity gate dielectric and metal gate electrodes for improved capacitive coupling between gate and channel
- Strained channel regions for carrier mobility enhancement

Cross-sectional TEM views of Intel’s 32nm CMOS devices
MOSFET Scaling Scenario

- Advanced MOSFET structures are anticipated to be needed to scale $L_g$ below ~20nm.
Why Multi-Gate FETs?

- SCE and DIBL are suppressed by using an adequately thin body, so channel/body doping can be eliminated.
  - higher $I_{ON}$ due to higher carrier mobility & improved gate control, reduced RDF-induced $V_T$ variation

![Diagram of FinFET and Tri-Gate structures with dimensions](https://via.placeholder.com/150)

**FinFET:**
- Body dimensions needed to suppress SCE

**Tri-Gate:**
- J. Fossum et al., *IEDM Tech. Dig.*, pp. 613-616, 2004
Carrier Transport in a MOSFET

What limits $I_{ON}$?

$L_{eff} >> \lambda$

Drift + Diffusion

$L_{eff} \sim \lambda$ (20nm for Si)

Quasi-Ballistic Transport

\[
I_D = W C_{ox} \nu_{sat} (V_{GS} - V_T)
\]

At high field: Saturation Velocity

At low field: Mobility

Injection Velocity (at source end)
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  N. Xu et al., SISPAD 2008
  – Acknowledgements: Xin Sun, Lynn Wang and Andrew Neureuther

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• Summary
Quasi-Ballistic Transport Model

A. Rahman et al., IEEE-TED Vol. 49, p.481, 2002

Total Current: 
\[ I_{\text{total}} = \frac{\sqrt{2} \beta \beta (\frac{\beta \beta \beta \beta}{\beta \beta})^3}{2 \hbar^2} \left(1 - \frac{\beta}{2} \left[ \mathcal{S}_{1/2} \left( \frac{\beta \beta}{\beta \beta} \right) - \mathcal{S}_{1/2} \left( \frac{\beta \beta \beta}{\beta \beta} \right) \right] \right) \]

Critical Length: 
\[ \ell_{\text{crit}} = \frac{E_{\beta}}{E_{\beta}} \left( \sqrt{\frac{E_{\beta} E_{\beta}}{E_{\beta} E_{\beta}}} \right) \] \[ \times \left( \frac{E_{\beta} E_{\beta}}{E_{\beta} E_{\beta}} \right)^{-1} \left( \sqrt{\frac{E_{\beta} E_{\beta}}{E_{\beta} E_{\beta}}} \right) \]

Backscattering Rate: 
\[ \beta = \frac{I_{\beta}}{I_{\beta} + \lambda_0} \]

Mean Free Path: 
\[ \lambda = \left( \frac{2 \beta \beta \beta \beta}{\beta \beta} \right) \mathcal{S}_0^2 \left( \frac{\beta \beta}{\beta \beta} \right) \times \mathcal{S}_{1/2} \left( \frac{\beta \beta}{\beta \beta} \right) \]
Modeling of Effective Channel Stress

1. Analytical model for stress distribution is calibrated using TCAD simulations

2. Average stress within the critical length region is calculated.

• Stress is modeled by a Gaussian function:

\[ S(x, L_g) = (L_g - L_0) \left\{ A_1 \exp \left[ -\frac{1}{2} \left( \frac{x}{L_g - L_0} \right)^2 \right] + A_2 \exp \left( -\frac{L_g}{L_0} \right) + A_3 \right\} \]

• \( l \) is dependent on drain bias.

→ Effective channel stress is dependent on drain bias.
Modeling of Strain Effects

**Energy Quantization**
Comparison of analytical model vs. Poisson-Schrodinger solution

(The 5 lowest conduction sub-bands hold 99% of the electrons.)

**Mobility**
Comparison of analytical model vs. piezoresistance model and exp. data

• Analytical model accounts for carrier redistribution and reduced inter-valley scattering.

**Effective Mass**

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Compact Modeling Flow

Drain bias → Critical Length

Stress profiles

Gate bias

Critical Length → Average stress in critical-length region

Average stress in critical-length region → Energy sub-band shifts, Effective mass changes

Energy sub-band shifts, Effective mass changes → Charge density, Surface Fermi level, Sub-band energies

Charge density, Surface Fermi level, Sub-band energies → Low-field mobility

Low-field mobility → Backscattering rate

Backscattering rate → Self-consistent solution

Self-consistent solution → Calculate $I_D$
Model Verification

40nm CESL-strained nMOSFET

S. Mayuzumi et al., IEDM Tech. Dig., p.293, 2007

• A good match to measured I-V data is achieved.
  Only 4 fitting parameters are needed.
Channel-Length Dependence

- The model well predicts the $L_g$ dependence of current enhancement

Future-Generation Devices

**Injection Velocity vs. Channel Length**

- Nanoscale MOSFETs will operate far below the ballistic limit.
- The benefit of stress diminishes with gate-length scaling.
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  N. Xu et al., IEDM 2010
  – Acknowledgements: Xin Sun; Wade Xiong and Rinn Cleavelin (TI)

• Summary
MuGFET Design Variations

- Fin aspect ratio, orientation, and stress configuration should be co-optimized for peak performance.

Fin Orientations

- A: S, D [100], [010], [001], [110]
- B: S, D [110], [110], [110], [110]

Stress Configurations

- a) Uniaxial Stress (CESL)
  - Sxx : Szz = 1 : -1
  - NMOS: Tensile
  - PMOS: Compressive
- b) Biaxial Stress
  - Sxx : Syy = 1 : 1
  - NMOS: Tensile
  - PMOS: Tensile & Compressive
- c) Transverse Stress (Metal Gate)
  - Syy : Szz = 1 : 1
  - Only transverse direction
  - Compressive
Inducing Strain in MuGFETs

Contact Etch Stop Liner (CESL)
TCAD simulations

Biaxial wafer bending

K. Uchida et al., IEDM Tech. Dig., 2004

Stress in CESL-FinFET

H_{Si} = 58nm
W_{Si} = 20nm
20nm-Thick CESL Initial Stress: 2GPa

S_{xx} sidewall
S_{xx} top
S_{yy} sidewall
S_{yy} top
S_{zz} sidewall
S_{zz} top

Electrical measurement equipment
Micrometer
Parallel ridges
Circular ridge

Stress vs micrometer knob

strain vs micrometer knob

0.11% ~ 200MPa
Simulation Approach

• To simulate the effect of transverse field and stress on carrier mobility, a 2-D Poisson-Schrödinger solver was developed to calculate the change in energy-band structure, accounting for quantum confinement.
  – For electrons, the effective mass approximation (EMA) is used, and non-parabolic E-k and stress effect on band structure are taken into account.
  – For holes, the 6×6 k•p approach is used, and the Pikus-Bir Hamiltonian is adopted for modeling stress effects.

![Carrier density profile with increasing gate bias](image)

• The Kubo-Greenwood formula is used to calculate low-field channel mobility, considering phonon and surface-roughness scattering.
Model Verification

Measured vs. simulated MuGFET Gate Capacitance

Calibrated Deformation and Scattering Parameters

<table>
<thead>
<tr>
<th>Electron Deform. Potential</th>
<th>Hole Deform. Potential</th>
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</thead>
<tbody>
<tr>
<td>$\Xi_u$ (eV)</td>
<td>$\Delta_{bs}$ (eV)</td>
</tr>
<tr>
<td>9.2</td>
<td>0.53</td>
</tr>
<tr>
<td>$\Xi_d$ (eV)</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>0.87</td>
<td>0.0189</td>
</tr>
<tr>
<td>$\Xi'_u$ (eV)</td>
<td>$\eta$</td>
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<tr>
<td>7</td>
<td>-0.809</td>
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</table>

<table>
<thead>
<tr>
<th>Electron Phonon</th>
<th>Hole Phonon</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{ac}$ (eV)</td>
<td>$a_v$ (eV)</td>
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<tr>
<td>14.7</td>
<td>2.1</td>
</tr>
<tr>
<td>$D_{IK}$ (eV/m)</td>
<td>$b$ (eV)</td>
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<tr>
<td>LO (g)</td>
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</tr>
<tr>
<td>1.1e11</td>
<td>TO (f)</td>
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<tr>
<td>0.2e11</td>
<td>0.2e11</td>
</tr>
<tr>
<td>$\hbar\Gamma$ (meV)</td>
<td>LA (f)</td>
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<tr>
<td>64</td>
<td>1.32e11</td>
</tr>
</tbody>
</table>

Surface Roughness

<table>
<thead>
<tr>
<th>(100) top</th>
<th>(100) sidewall</th>
<th>(110) sidewall</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta$ (Å)</td>
<td>4.8(e) 3.6(h)</td>
<td>6.6(e) 4.2(h)</td>
</tr>
<tr>
<td>$L$ (Å)</td>
<td>10(e) 26(h)</td>
<td>10(e) 22(h)</td>
</tr>
</tbody>
</table>

A good match to measured C-V data is achieved.
MuGFET Effective Mobility

- Good agreement is seen between experiment and simulation:

**Electron Mobility**

- In FinFET: sidewall surfaces dominate
- In Tri-Gate FET: top surface dominates, and is of higher quality
Mobility Change with Biaxial Stress

- NMOS: Enhancement decreases due to carrier redistribution.
- PMOS: Reduction in enhancement is less remarkable.
Comparison of Stress Configurations
FinFET Electron Mobility

• $\mu_n$ is more sensitive to stress for a <110>-oriented fin.
• CESL provides the most enhancement, via a reduction in effective mass.
Comparison of Stress Configurations
FinFET Hole Mobility

- \( \mu_p \) is more sensitive to stress for a \(<110>\)-oriented fin.
- CESL provides the most enhancement, via reductions in effective mass and scattering rate.
FinFET vs. Tri-Gate FET Comparison

Electron Mobility

- Open: FinFET
- Filled: Tri-Gate

Hole Mobility

- Open: FinFET
- Filled: Tri-Gate

- CESL Compressive
- Biaxial Compressive
- Biaxial Tensile

• NMOS: <100> Tri-Gate FET is the best
• PMOS: <110> Tri-Gate FET is the best for high stress levels >600MPa
Simulated Carrier Thermal Velocity (FinFET)

- CESL-induced stress can provide for large enhancements
Extraction of Short-Channel MuGFET Mobility and Injection Velocity

- Linear region mobility extraction
  - Y-function approach $\rightarrow V_{th}$ and $R_{S/D}$
  - split-CV measurement $\rightarrow L_{eff}$
  $\rightarrow$ Impact of ballistic transport on $\mu$

- ON-state injection velocity extraction
  - DIBL measurement $\rightarrow dV_{th}$
  - Inversion charge:
    $$ q_{inv} = \int_0^{V_{gs}'} C_{gsd} dV_{gs}'; \quad V_{gs}' = V_{gs} - I_{ds} R_s $$
  - Injection velocity:
    $$ v_{inj} = \frac{I_{on}}{WQ_{inv}} $$
  $\rightarrow$ Dependence of $v_{inj}$ on $\mu$
Extracted Short-Channel FinFET Mobility

- Degradation seen with decreasing $L_{\text{eff}}$, due to ballistic transport
- Extracted values are much lower than simulated, due to strong Coulomb scattering from defects.
Extracted Short-Channel FinFET Injection Velocity

**NMOS**

- \( \mu_{\text{eff}} / L_{\text{eff}} \) (10^7 cm/V.s)
- \( L_{\text{eff}} = 56.6\text{nm} \)
- \( v_{\text{inj}} / v_{\text{bal}} = 57.68\% \)

**PMOS**

- \( \mu_{\text{eff}} / L_{\text{eff}} \) (10^7 cm/V.s)
- \( L_{\text{eff}} = 56.6\text{nm} \)
- \( v_{\text{inj}} / v_{\text{bal}} = 54.35\% \)

- Injection velocity depends largely on apparent mobility.
- (40% to 50% ballistic, similar as for bulk MOSFETs)
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Summary

• $I_{ON}$ in nano-scale MOSFETs is limited by the carrier injection velocity, which can be predicted by a physically-based compact model.
  → Enables projections of performance/delay at future nodes

• To maximize MuGFET $I_{ON}$, fin orientation and aspect ratio should be co-optimized for the chosen stressor.
  - CESL will be the most effective stressor for MuGFETs.

• Defect-induced Coulomb scattering has a strong impact on apparent mobility and injection velocity.
  → A new challenge to realizing the full benefit of strain
Acknowledgements

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