Schottky-Barrier Engineering for Low-Resistance Contacts

Pankaj Kalra, Hideki Takeuchi, Tsu-Jae King

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA

Oct 03, 2005
Outline

• Introduction
• Characterization Schemes
• $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain
• Dopant Segregation
• Strain
• Summary
Parasitic Resistance Components

- $R_{sl}$ Silicide sheet resistance
- $R_{csd}$ Contact Resistance
- $R_{sd}$ Silicon Sheet Resistance
- $R_{ov}$ Overlap resistance

- Parasitic resistance must be $<10\%$ of total FET resistance
- CMOS scaling
  - reduces channel resistance $\propto 1/L$
  - increases contact resistance

Source: Prof. Jason Woo, UCLA
Contact Resistance Scaling

- Change in contact scheme (adoption of SALICIDE) has extended the contact scaling
- Due to the reduction of active area, silicide/Si contact resistance is now an issue
Int’l Technology Roadmap for Semiconductors (2004 update)

- New materials and processes are needed
Impact of $R_c$ on FinFET

H. Kam and T.-J. King, 2004 Silicon Nanoelectronics Workshop

$L_{gate} = 18$ nm, $L_{eff} = 22$ nm

- Parasitic resistances dominate FinFET performance
- $\rho_c < 10^{-8} \, \Omega\text{-cm}^2$ required

$V_{ds}$

$I_{ds}$

Wrapped Contact, $\rho_c = 0$

Wrapped Contact

End Contact

Top Contact

16% reduction

34% reduction

$\rho_c = 10^{-8} \, \Omega\text{-cm}^2$
Specific Contact Resistivity
Barrier Height and Active Dopant Concentration

\[ R_{co} = \frac{\rho_c}{A_c} \]

\[ \rho_c \propto \exp\left(\frac{4\sqrt{\varepsilon m^*}}{\hbar} \frac{\phi_B}{\sqrt{N}}\right) \]

- Dopant concentration, \( N \)
- Barrier height, \( \phi_B \)

- Fermi-level pinning results in:
  - Barrier height independent of metal work function
Approaches to Lowering $\rho_c$

- **Material engineering**
  - SiGe source/drain  
    - smaller bandgap $\rightarrow$ smaller Schottky barrier
    - $\rho_c \sim 10^{-8}$ $\Omega$-cm$^2$ for Ni germanosilicides on SiGe
  - lower resistivity

- **Barrier height tuning**
  - image force lowering by dopant segregation
    - A. Kinoshita et al., *Symp. VLSI Technology*, 2004
  - strain-induced $\phi_B$ reduction
    - A. Yagishita et al., *SSDM*, 2003

- **Fermi-level de-pinning by interface engineering**
  - insertion of insulator layer
  - selenium passivation
    - M. Tao et al., *APL*, 2003
Research Objective

• To understand the mechanisms for tuning the effective Schottky barrier height of a metallic electrode, to guide the engineering of contact-formation processes
  – Low-$\phi_B$ contacts for reduced parasitic resistance
  – Demonstrate fully silicided source/drain UTB MOSFETs with improved $I_{dsat}$ by reducing $\rho_c$ (to $<10^{-8} \Omega\text{-cm}^2$) for silicide-to-silicon contacts
Outline

• Introduction

• Characterization Schemes
  • $\text{Si}_{1-x}\text{Ge}_x$ Source/ Drain
  • Dopant Segregation
  • Strain

• Summary
Minimum measurable resistance is $\sim 10 \, \Omega$

$\Rightarrow$ Need very small contact holes to determine $\rho_c$ accurately below $10^{-8} \, \Omega \cdot \text{cm}^{-2}$
Test structures

- Fabrication of Kelvin structures
  - Evaluation of contact resistance

- Fabrication of diode
  - Measure schottky barrier height
Fabrication of Sub-0.25µm Contacts

- Contacts were fabricated using DUV stepper ASML5500/90; Cymer KrF excimer laser (λ=248nm)

<table>
<thead>
<tr>
<th>Energy (mJ/cm²)</th>
<th>After Litho (nm)</th>
<th>After Etch (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>65</td>
<td>188</td>
<td>171</td>
</tr>
<tr>
<td>70</td>
<td>247</td>
<td>211</td>
</tr>
<tr>
<td>75</td>
<td>261</td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>268</td>
<td></td>
</tr>
<tr>
<td>85</td>
<td>275</td>
<td></td>
</tr>
</tbody>
</table>
**$\phi_B$ extraction**

- Measure diode $I-V$ characteristic at different temperatures

\[
\ln\left(\frac{I_F}{T^2}\right) \approx \ln\left(A_e A^{**}\right) - \frac{q}{kT}\left(\phi_{Bn} - V_F\right)
\]

10/03/05
Outline

• Introduction

• Characterization Schemes

• Si_{1-x}Ge_x Source/ Drain
  (This work is sponsored by the FLCC project)

• Dopant Segregation

• Strain

• Summary
Dopant Behavior in Ultra-Thin SOI

- P-channel thin-body FETs exhibit higher series resistance

→ Different behaviors of B and P in ultra-thin Si
  - dopant segregation to interface(s), or into surrounding oxide?
Epitaxial $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain

- Epitaxial $\text{Si}_{1-x}\text{Ge}_x$ source/drain regions for lowering $R_{\text{series}}$ and inducing compressive strain to enhance hole mobility
  - Conventional approach for epitaxial growth of $\text{Si}_{1-x}\text{Ge}_x$ is not possible for thin-body devices because there is not sufficient crystalline substrate after S/D etchback
Approach

- Develop a process for selectively forming strained $\text{Si}_{1-x}\text{Ge}_x$-in-SOI by intermixing Ge & Si
  - Study the intermixing of Ge with SOI films
    - effects of anneal temperature, time, boron doping
  - Investigate strain in the resultant $\text{Si}_{1-x}\text{Ge}_x$ alloy
  - Characterize metal-to-$\text{Si}_{1-x}\text{Ge}_x$ contact resistance
  - Germano-silicidation of $\text{Si}_{1-x}\text{Ge}_x$ to achieve dopant pile-up (to study $\phi_B$ reduction)
Advantages of This Approach

- Selective deposition of Ge by conventional LPCVD
  - GeH$_4$ gas, 320°C, 200mT
  - high process throughput (batch process)

\[ \rightarrow \text{low cost} \]

XTEM of UTB MOSFET w/ raised Ge S/D

Ge/Si Interface Preparation

• Selective Ge deposition in LPCVD furnace requires a clean silicon surface
  – Interface preparation is critical

• Native oxide removal methods
  – *in-situ* HF vapor clean
  – *in-situ* HF vapor clean and Hydrogen bake
  – HF dip followed by Hydrogen bake
  – *in-situ* cleaning by GeH₄
  – Si I/I after Ge deposition
    • for breaking up any native oxide at the Ge/Si interface
In-Situ GeH₄ Cleaning

 Decreased GeH₄ flow to diffuse Ge on the surface

Clean surface

Si Ion Implantation to Break Up Native Oxide

- Si$^+$ implant has been used to break up the native oxide barrier for Solid-Phase Epitaxy (SPE)

Test Sample Process Flow

• Starting wafers
  – n-type, $\rho=5\text{-}10 \ \mu\Omega\text{-cm}$

• Cross-sectional TEM pattern formation
  – CVD SiO$_2$ deposition (52nm)
  – Lithography
  – Oxide etching (90% dry + 10% wet)
Process Flow (Cont’d)

• Interface Preparation
  – HF last / HF vapor

• Selective Ge deposition (22nm)
  – 320°C/200mTorr/100sccm
  – Capping layer (25nm)

• Si Implant
  – Si : 40keV, 1E15 cm⁻²

• Doping
  – B : 10keV, 2E15 cm⁻²

• Recrystallization
  – 500°C, 1 hour

• Intermixing anneal
  – 800°C/ 850°C, 1minute
Experimental Splits

on wafer splits = 4

Split Table:

<table>
<thead>
<tr>
<th>Wafer ID</th>
<th>Cleaning</th>
<th>I/I splits</th>
<th>Annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HF Last</td>
<td>Si I/I</td>
<td>800 C</td>
</tr>
<tr>
<td></td>
<td>HF vapor</td>
<td>Si I/I + B I/I</td>
<td>800 C</td>
</tr>
<tr>
<td></td>
<td>none</td>
<td>B I/I</td>
<td>800 C</td>
</tr>
<tr>
<td></td>
<td>none</td>
<td>Si I/I + B I/I</td>
<td>850 C</td>
</tr>
<tr>
<td></td>
<td>none</td>
<td>none</td>
<td>850 C</td>
</tr>
<tr>
<td></td>
<td>B I/I</td>
<td>Si I/I + B I/I</td>
<td>850 C</td>
</tr>
<tr>
<td></td>
<td>none</td>
<td>none</td>
<td>850 C</td>
</tr>
</tbody>
</table>
Determining Ge and B profiles
(in collaboration with Prof. Haller’s group)

• Characterization of vertical and lateral co-diffusion of Ge and B
  – Available Options:
    • Cross-sectional TEM with EDX nanoprobe
    • Cross-sectional TEM with EELS
    • Cross-sectional SEM with EDX nanoprobe
Summary and Future Goals

\textbf{Si}_{1-x}\text{Ge}_x \text{ Source/Drain}

• Fabrication of first batch is finished
  – Splits for Doped/ undoped Ge, interface preparation, annealing conditions etc.
  – Results of this batch are awaited

• Future Work:
  – Characterization of boron-doped \text{Si}_{1-x}\text{Ge}_x-on-insulator resistance
  – Characterization of metal-to-\text{Si}_{1-x}\text{Ge}_x contact resistance
    • Germano-silicidation of \text{Si}_{1-x}\text{Ge}_x to achieve dopant pile-up for Schottky barrier height $(\phi_B)$ reduction
Outline

• Introduction
• Characterization Schemes
• $\text{Si}_{1-x}\text{Ge}_x$ Source/ Drain
• **Dopant Segregation**  (This work is sponsored in part by Intel Corp.)
• Strain
• Summary
**$\phi_B$ Reduction by Dopant Segregation**

- $\phi_B$ can be reduced by using an ultrathin (<10nm) heavily doped layer at the semiconductor surface


  - Image force lowering ($\Delta\phi$) due to surface electric field

  $$\Delta\phi = \frac{q}{\varepsilon_{si}} \sqrt{\frac{N a}{4\pi}}$$

  $N =$ dopant concentration in surface layer
  $a =$ width of heavily doped surface layer

Such a thin heavily doped layer can be formed by silicidation-induced dopant segregation:

Experiment

**Goals:** Confirm dopant segregation w/ NiSi
Investigate dopant activation

Process sequence:
- starting Si wafer (n-type/ p-type)
- deposit capping layer, CVD SiO₂
- blanket implantation
  (B- 20KeV, 10¹⁶cm⁻²  As- 80KeV, 6×10¹⁵cm⁻²)
- spike annealing@1000C
- strip capping layer
- excimer laser annealing
- Ni deposition
- silicidation
- strip unreacted Ni
Results: SIMS Analyses

- Dopant pile-up at silicide/Si interface is seen for both As and B doping (only As shown here)
**Schottky Barrier Lowering**

- Image Force Effect
  - Induced charges at the interface
  - Equivalent to an image charge

\[
qE_g = qE_{\text{v}}(x) = qE_{\text{F}} = q\psi(x)
\]

\[
x_m = \sqrt{\frac{q}{16\pi \varepsilon_s E}}
\]

\[
PE(x) = -\frac{q^2}{16\pi \varepsilon_s x} - qE_x
\]

\[
\Rightarrow \Delta\phi = \sqrt{\frac{q}{4\pi \varepsilon_s \sqrt{E}}}
\]
Tailoring the Surface Electric Field

\[ \Delta \phi \] depends on the surface electric field
- Lightly doped substrate:
  • Low \( E \), barrier-lowering is sensitive to reverse bias
- Heavily doped substrate:
  • High \( E \) \( \Rightarrow \phi_B \) is reduced, but reverse current increases
    \( \Rightarrow \) tunneling Ohmic contact!

• To retain Schottky junction properties and to achieve \( \Delta \phi \) that is insensitive to bias, a heavily doped surface layer that is *fully depleted by the built-in potential* is needed
Fully-Depleted Doped Surface Layer

• The required electric field has been shown to be $>5 \times 10^5 \text{ V/cm}$


  – Maximum surface field arising from implantation of a symmetrical distribution of charge about range $R_p$:

\[
E_{s,\text{max}} \approx \frac{V_b}{R_p}
\]

\[
qV_b = q\phi_{B0} - (E_c - E_f)
\]

For a metal contacting a lightly doped substrate, built-in potential $V_b \sim 0.45V$

\[
\Rightarrow R_p < 100 A
\]
**Φ_B Reduction Model**

- Maximum surface field, $E_{s,max}$

\[
E_{s,max} = \frac{q}{\varepsilon_s} [N_p a + N_B (W - a)]
\]

\[
E_{s,max} \approx \frac{q}{\varepsilon_s} N_p a
\]

\[
\Rightarrow \Delta \phi \approx \frac{q}{\varepsilon_s} \sqrt{\frac{N_p a}{4\pi}}
\]

Expected barrier height lowering due to a thin highly doped surface layer:
Effect of Interface States

- Metal-induced gap states (MIGS)
  - Penetration of wave function from the metal into the forbidden energy gap of Si

Electron potential energy including the contributions of image force and MIGS


\[ PE(x) = -\frac{q^2}{16\pi\varepsilon_s x} - qE_x - \frac{qQ\lambda}{\varepsilon_s} e^{-\frac{x}{\lambda}} \]

- \( Q \) = magnitude of surface state charge
- \( \lambda \) = penetration depth of surface state charge
**Δφ Inverse Modeling Approach**

- Find the location of $PE(x)$ minimum

$$\left. \frac{d}{dx}(PE(x)) \right|_{x=x_m} = 0 \quad \Rightarrow \quad \frac{q^2}{16\pi\varepsilon_s x_m^2} qE(x_m) + \frac{qQ}{\varepsilon_s} e^{-x_m/\lambda} = 0$$

- Total barrier lowering is given by

$$\Delta \phi = \frac{q}{16\pi\varepsilon_s x_m} - \psi_0(0) - \psi_0(x_m) + \frac{Q\lambda}{\varepsilon_s} e^{-x_m/\lambda}$$

- Solve Poisson’s equation to find $\Psi_0(x)$

$$\nabla^2 \psi_0(x) = - \frac{\rho(x)}{\varepsilon_s}$$

- Extract $Q$ and $\lambda$ from measured forward $I-V$ characteristics

- Predict total barrier lowering from the model
  - $N_p$, work-function difference, $Q$, and $\lambda$ are input parameters
Determining Active Dopant Concentration

• Spreading Resistance Probe (SRP):
  – within 1/2 the probe spacing (~10µm) of the Si/ silicide interface, silicide starts affecting readings because of low resistance

→ Need to remove NiSi selectively
  • surface roughness increase
  • difficult to find bevel edge
Summary and Future Work

Dopant Segregation

• Ni silicidation induced dopant segregation phenomenon confirmed

• A quantitative inverse-modeling approach has been established for determining the amount of Schottky-barrier lowering

• Future Work:
  – Fabrication and characterization of diode structures and Kelvin structures
  – Application of dopant-segregation technique to improve FinFET performance by reducing S/D contact resistance
Outline

• Introduction
• Characterization Schemes
• $\text{Si}_{1-x}\text{Ge}_x$ Source/ Drain
• Dopant Segregation
• Strain
• Summary
$\phi_B$ Reduction by Si Strain

A. Yagishita et al., SSDM 2003

- 1% bi-axial strain reduces $\phi_B$ by 0.1eV (ErSi$_{1.7}$ S/D NMOSFET)
Experimental Plan

• Use a bending apparatus
  – apply uniaxial or biaxial bending stress to Si chips

• Study $\phi_B$ reduction
  – Fabricate Schottky diodes and contact test structures to measure effect of strain on $\rho_c$

K. Uchida et al., IEDM 2004
Outline

• Introduction
• Characterization Schemes
• $\text{Si}_{1-x}\text{Ge}_x$ Source/ Drain
• Dopant Segregation
• Strain
• Summary
Summary

• Source/drain contact resistance can limit the performance of nanoscale FETs
  – $\rho_c \sim 10^{-9} \, \Omega \cdot \text{cm}^2$ will be required

• Approaches for reducing $\rho_c$ include use of $\text{Si}_{1-x}\text{Ge}_x$ in the source/drain regions, dopant segregation, and strain

• Work in progress will clarify the mechanisms for lowering the effective Schottky barrier height $\phi_B$
  → Application to nanoscale thin-body FETs
Acknowledgements

• Akira Hokazono (Toshiba Corporation)
• Dr. Chi On Chui (Intel Corporation)

• Research funding from
  – UC Discovery Grant program and member companies of the Feature-Level Compensation and Control (FLCC) project at UC-Berkeley
  – Intel Corporation