# Segmented MOSFET Technology for Reduced Variability

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*IMPACT Project Seminar*

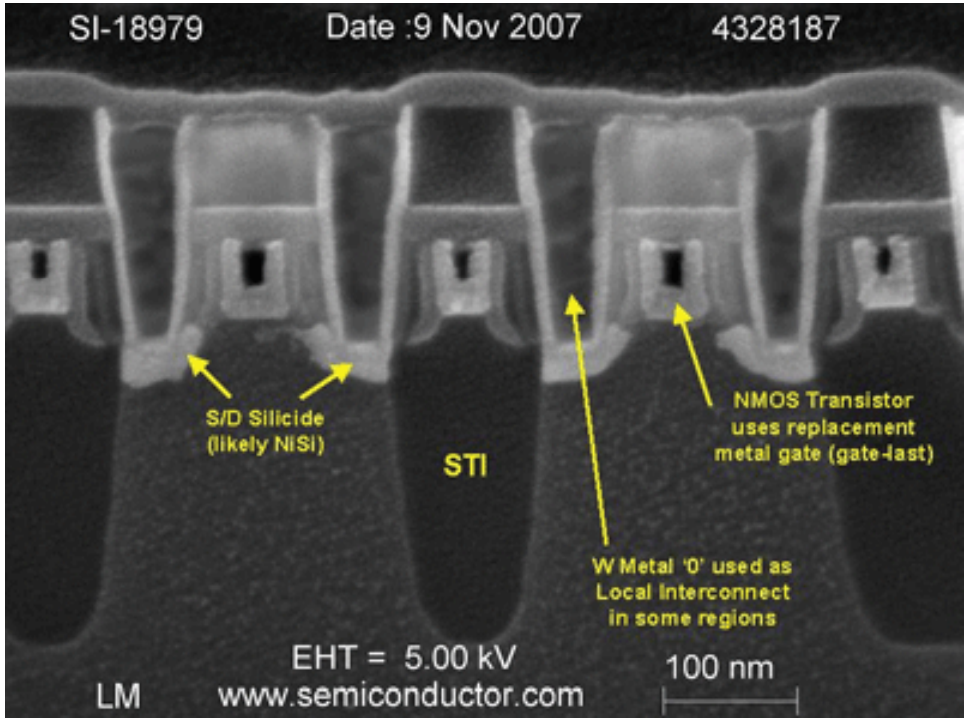
# Outline

- Introduction
  - Transistor scaling challenges
  - Advanced transistor structures
- Tri-Gate Bulk/PD-SOI FET Design
- Corrugated Substrate Technology
- Summary

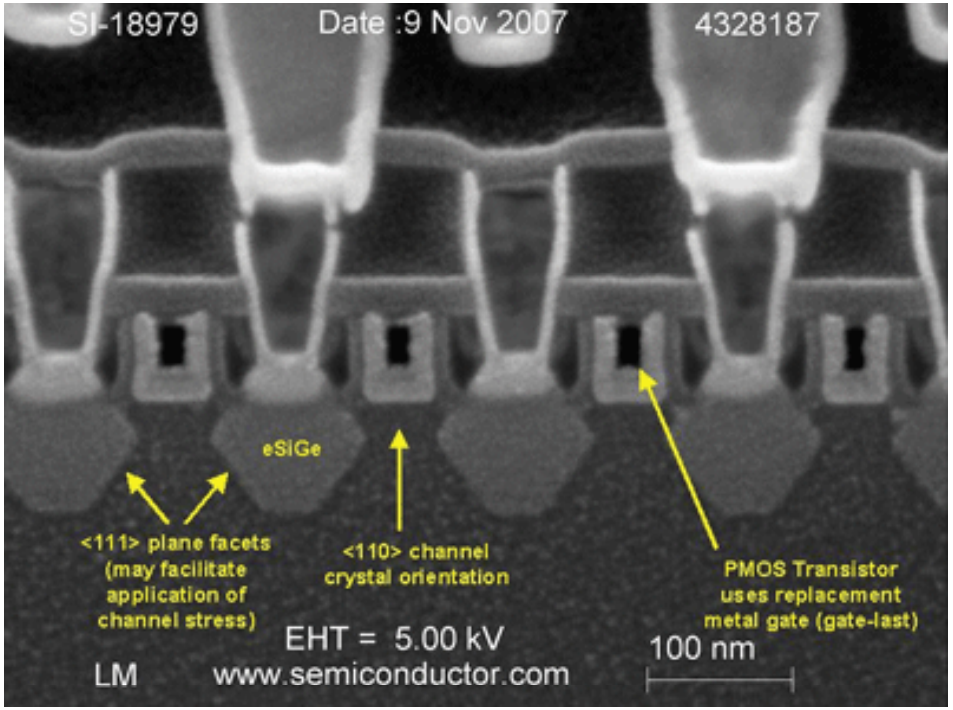
# Modern MOSFET Structures

**(Intel Penryn©, from www.semiconductor.com)**

**N-channel MOSFETs**



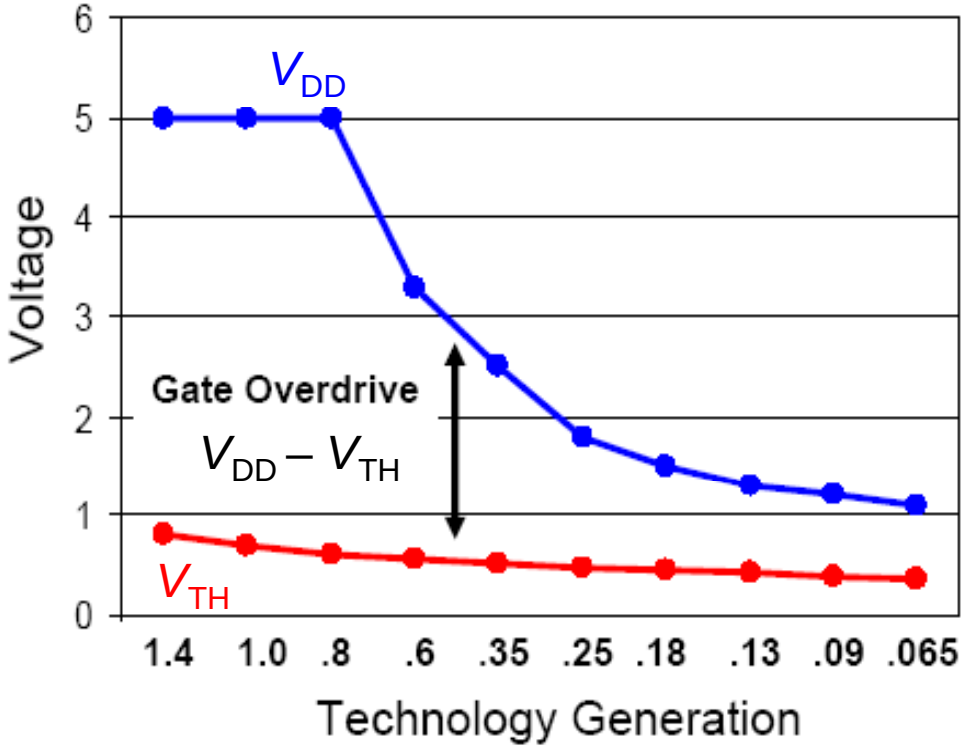

**P-channel MOSFETs**



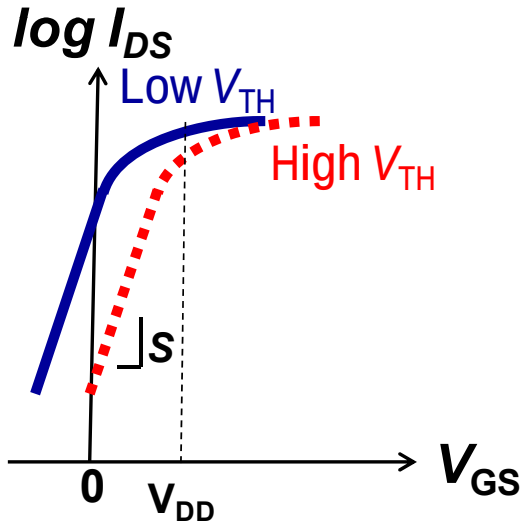

- **45nm CMOS technology features:**
  - **high-permittivity gate dielectric and metal gate electrodes**
  - **strained channel regions**
  - **aggressive silicidation of n+ source/drain regions**

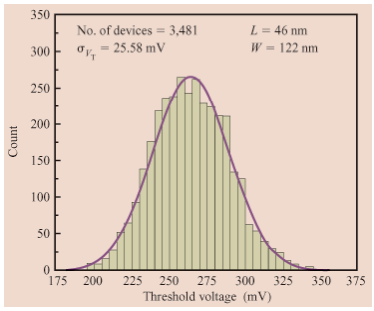
# Historical Voltage Scaling

- **Since the threshold voltage $V_{TH}$ cannot be scaled down aggressively, the power-supply voltage ($V_{DD}$) has not been scaled down in proportion to the MOSFET gate length:**




Source: P. Packan (Intel), 2007 IEDM Short Course

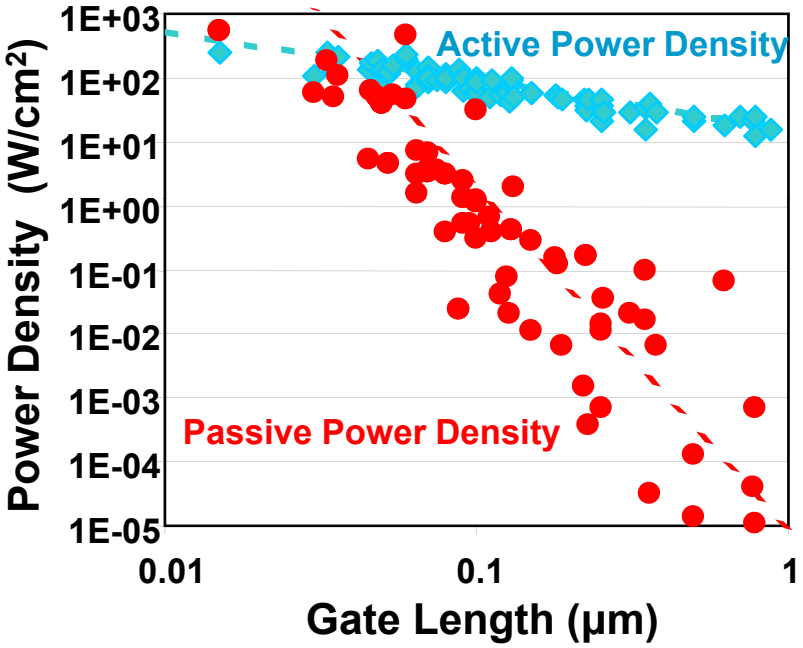



K. Bernstein *et al.*, *IBM J. Res. Dev.* 50-4/5, 2006:

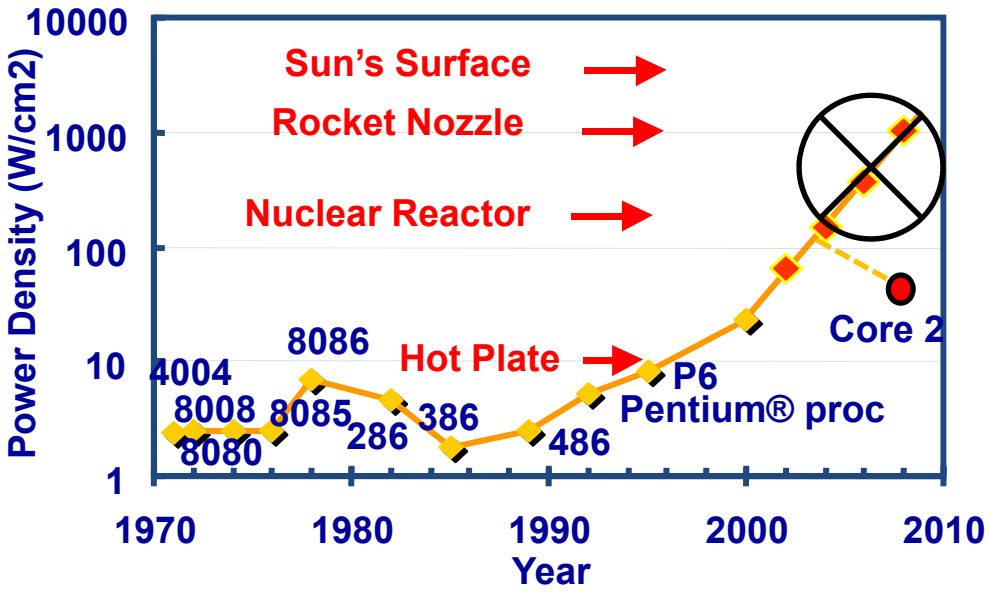
# The CMOS Power Crisis

**Power Density vs. CMOS Scaling**




Source: B. Meyerson (IBM) Semico Conf., January 2004

**Power Density Prediction circa 2000**

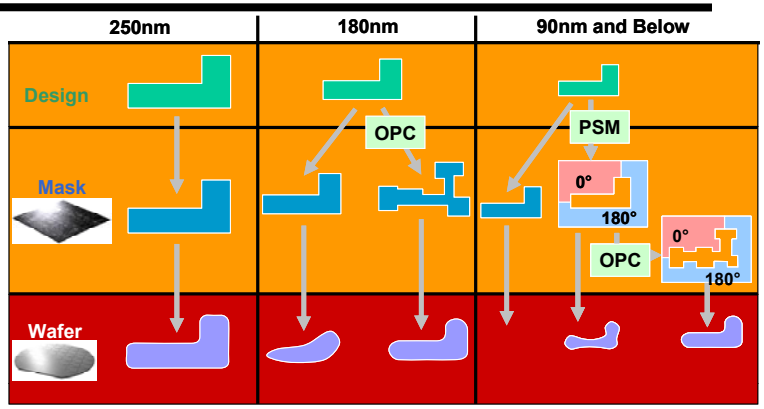



Source: S. Borkar (Intel)

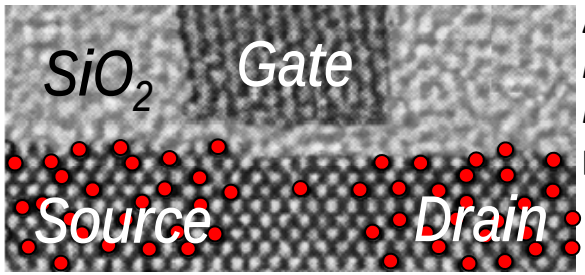
- **Improved MOSFET design for lower leakage and reduced variability eventually will be needed to mitigate this crisis.**

# Sources of Variability

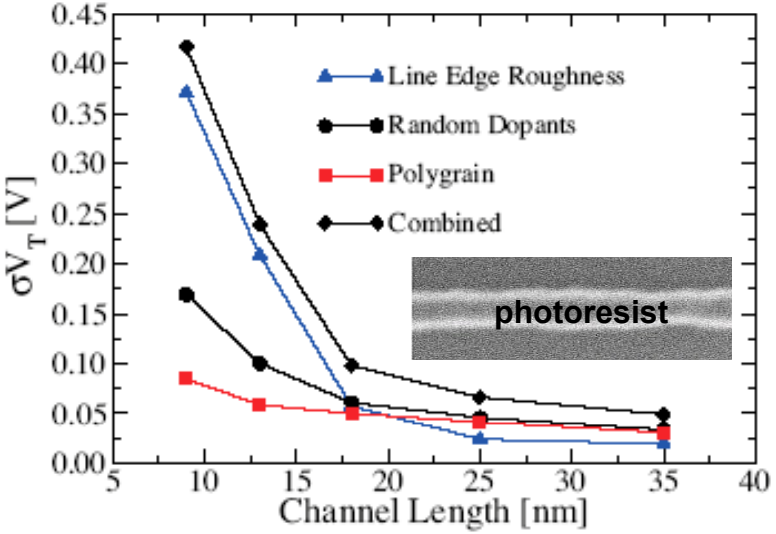
- **Sub-wavelength lithography:**
  - **Resolution enhancement techniques are costly and increase process sensitivity**




- **Layout-dependent transistor performance:**
  - **Process-induced stress is dependent on layout**
- **Random dopant fluctuations (RDF):**
  - **Atomistic effects become significant in nanoscale FETs**



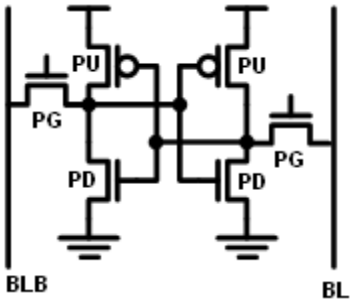

A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002




A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

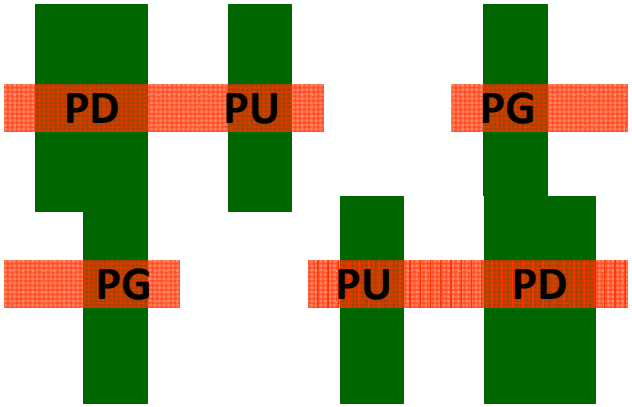
- **Random Telegraph Noise (RTN)**

6-T SRAM Cell

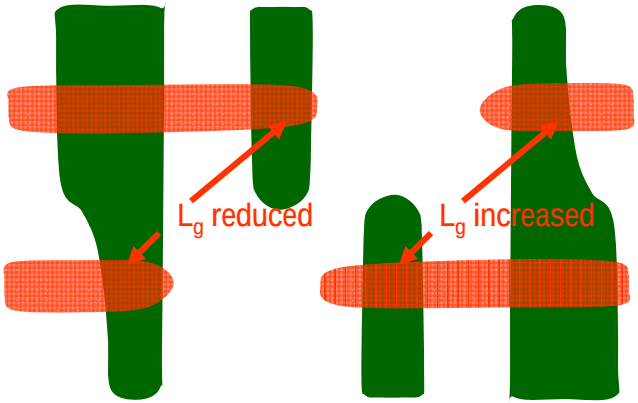



# Impact of Misalignment

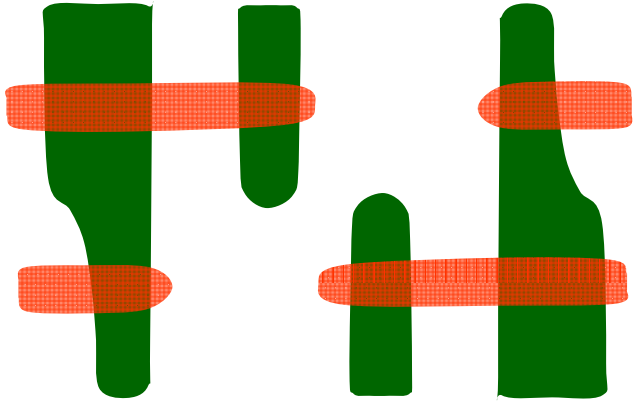
**Desired layout**
**(6-T SRAM cell)**



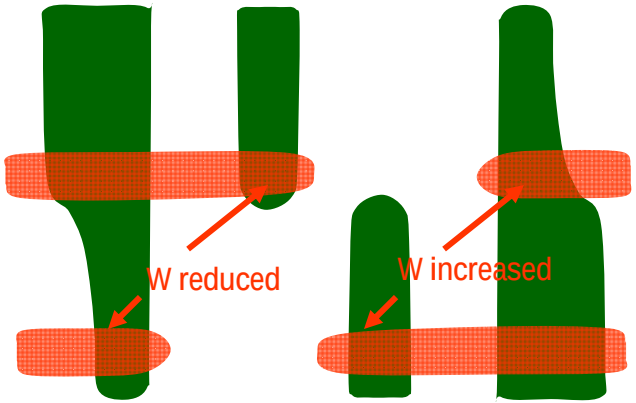

**Actual layout w/ lateral misalignment**
**(gate length variations)**



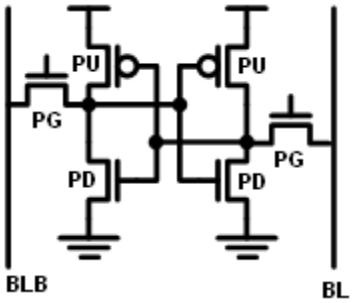

**Actual layout**
**(corner rounding)**



**Actual layout w/ vertical misalignment**
**(channel width variations due to active jogs)**

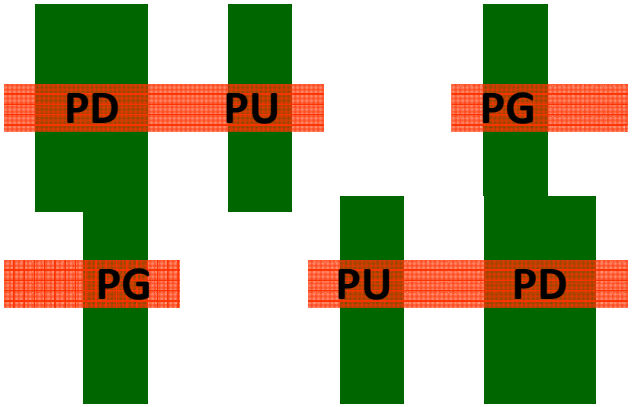


6-T SRAM Cell

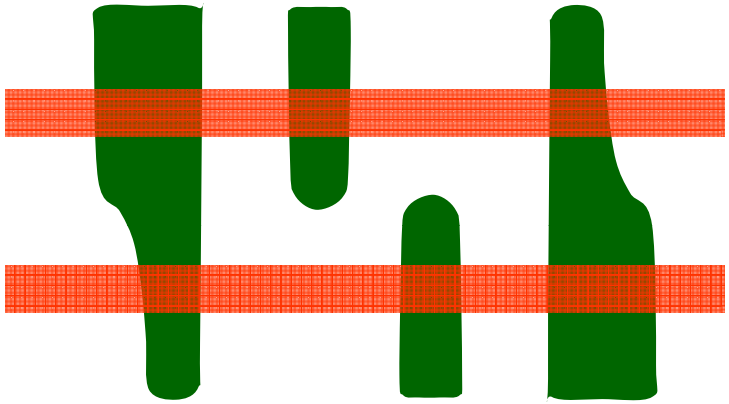



# Double Patterning of Gate

Desired layout
(6-T SRAM cell)

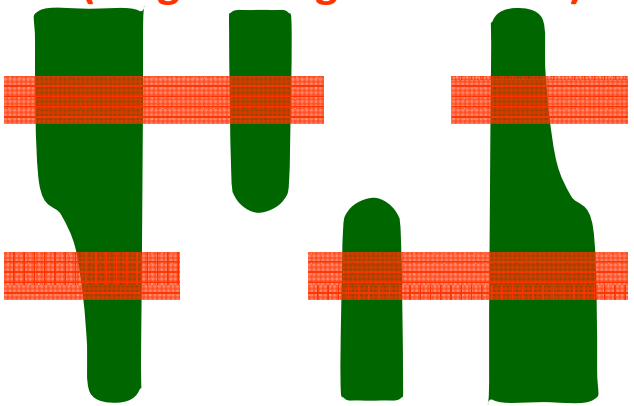



Actual layout after 1st gate patterning



Actual layout after active patterning

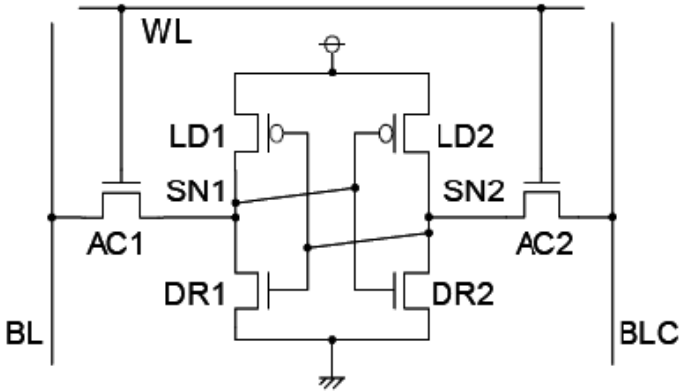
Actual layout after 2nd gate patterning
(no gate length variation)



# Impact of Variability on SRAM

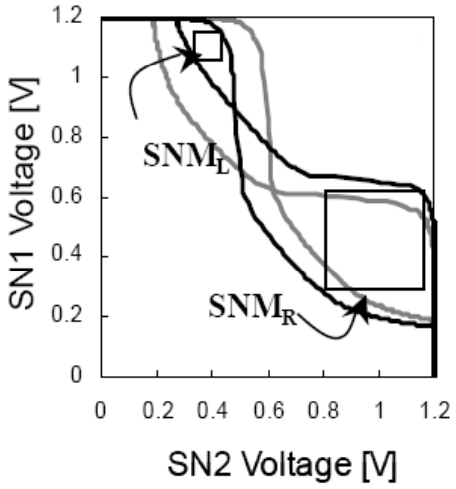
- $V_{TH}$ mismatch results in reduced static noise margin.
  → lowers cell yield, and limits $V_{DD}$ scaling

**Circuit Schematic of 6-T SRAM Cell**




Y. Tsukamoto *et al.*, *Proc. IEEE/ACM ICCAD*, p. 398, 2005

**Butterfly Curve**



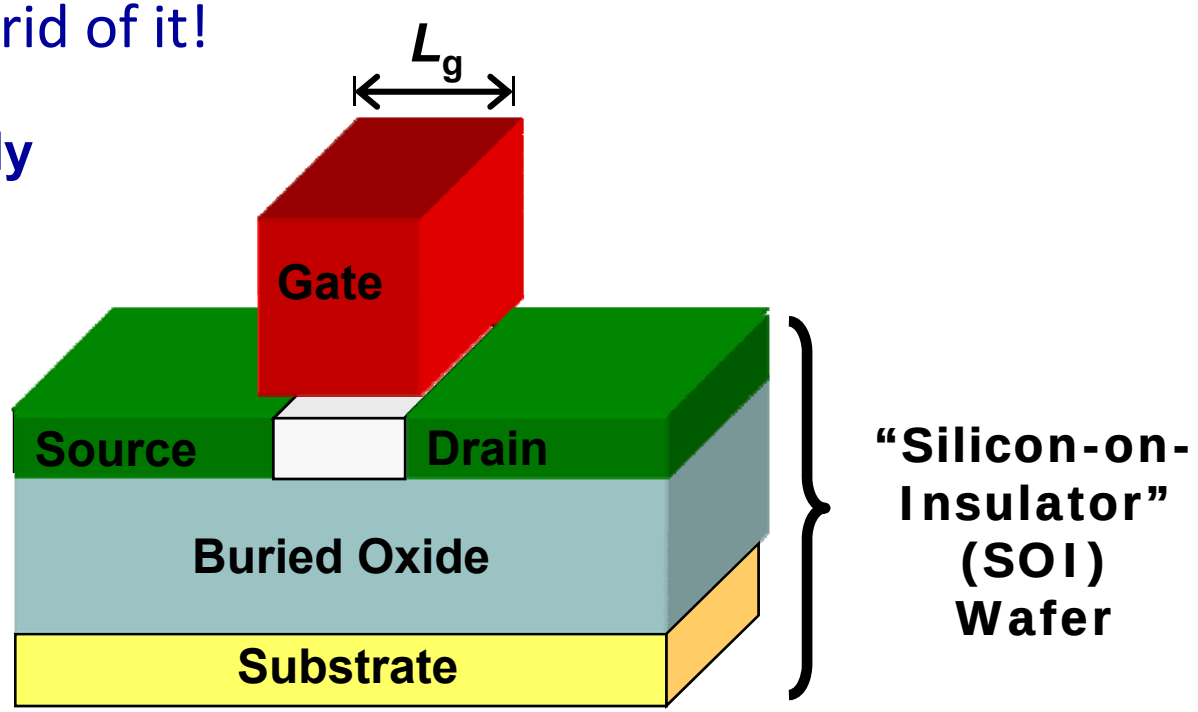

→Immunity to short-channel and narrow-channel effects, as well as RDF effects, is needed to achieve high SRAM cell yield.

# Why New Transistor Structures?

- **Leakage must be suppressed as $L_g$ is scaled down**
- **Leakage occurs in the region away from the channel surface**

→ Let's get rid of it!

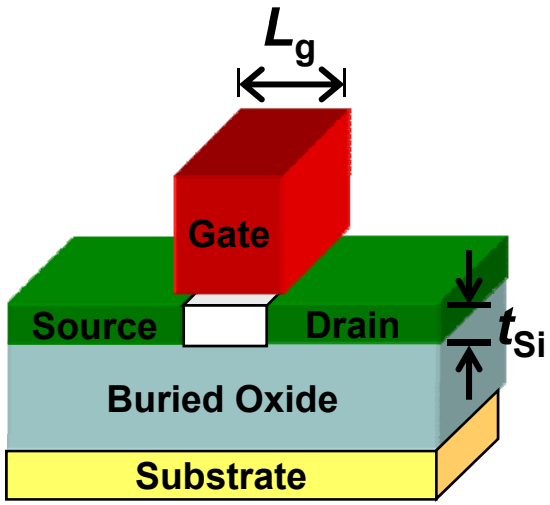
**Thin-Body MOSFET:**



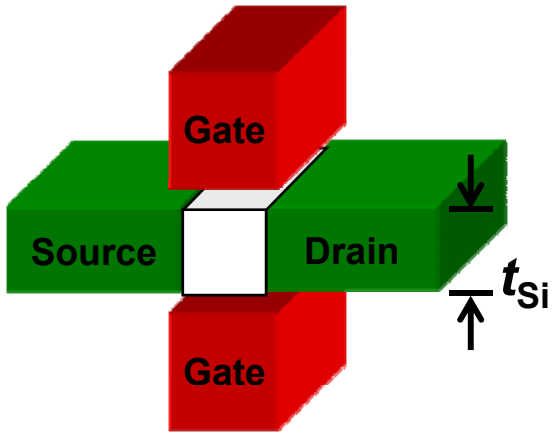
# Thin-Body MOSFETs

- **Leakage can be suppressed by using a thin body** ($t_{Si} < L_g$)
  - Channel doping is not needed → higher carrier mobility
  - Aggressive gate-oxide scaling is not needed
- **The double-gate structure is more scalable** (to $L_g$<10nm)

**Ultra-Thin Body (UTB)**

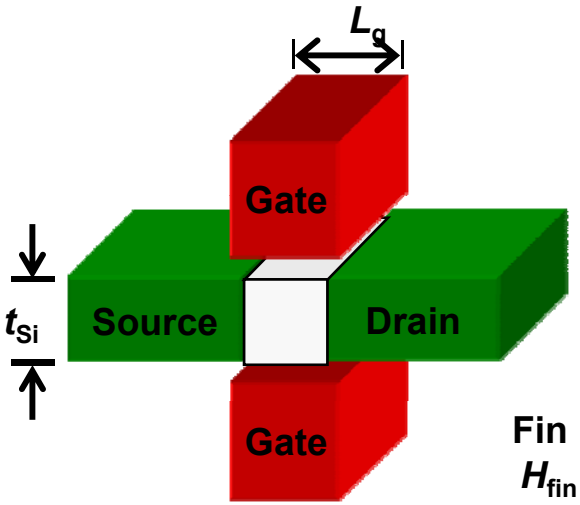



**Double-Gate (DG)**

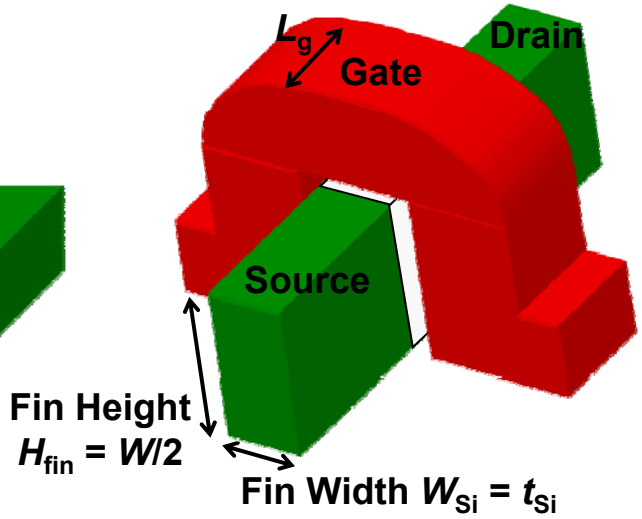


# Vertical Double-Gate "FinFET"

**Planar DG-FET**

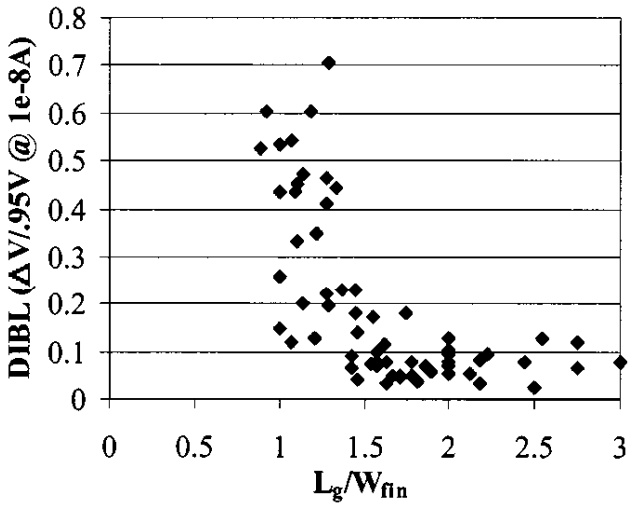



**FinFET**

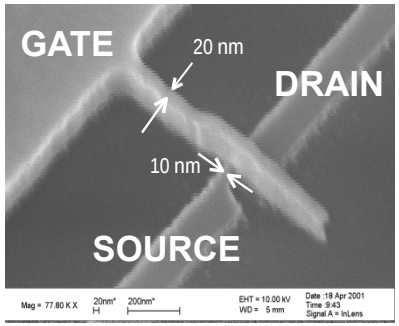



D. Hisamoto et al., *IEEE Int'l Electron Devices Meeting*, 1998

N. Lindert et al., *IEEE Electron Device Letters*, p.487, 2001




**15nm $L_g$ FinFET:**

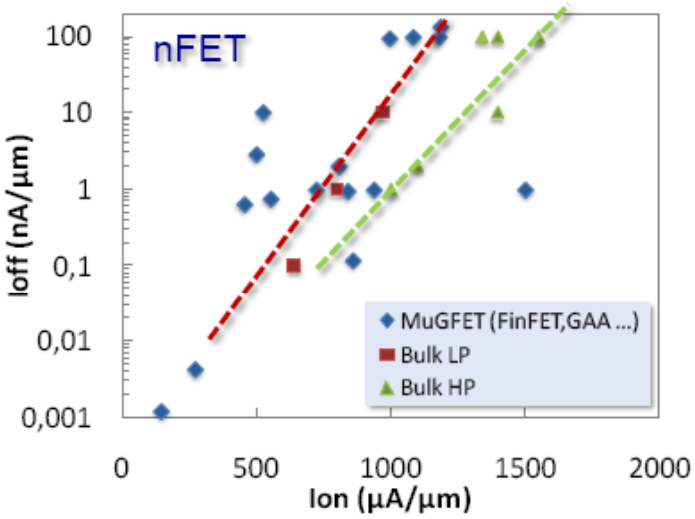


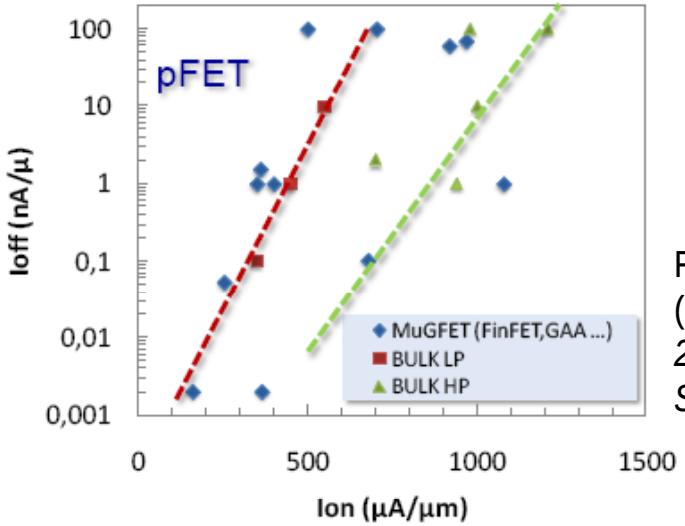

Y.-K. Choi et al., *IEEE Int'l Electron Devices Meeting* 2001

# Thin-Body MOSFET Challenges

- **"There are various problems associated with a move to multi-gate field-effect transistors (MuGFETs)…challenges with parasitic resistance, parasitic capacitance and vertical topology will make MuGFETs difficult to implement."**

K. Kuhn (Intel Fellow, Director of Advanced Technology) in *EE Times*,12/15/08




F. Boeuf
(ST Microelectronics),
*2009 Symp. VLSI Technology Short Course*

- **For LP applications , MuGFET are competitive (or exceed) state of the art Bulk logic performance**
- **For HP application, no clear improvement is evidenced**

Y. Jiang VLSI 2008, p.34
K.H.Yeao et al., IEDM 2006, p.539
N. Singh et al. IEDM 2006, p.547
H. Lee et al., VLSI 2006, p.58
F.-L. Yang et al, VLSI 2004, p196
Y. Tian et al., IEDM 2007, p695
S.D. Suk et al., IEDM 2005, p717
W. W. Fang et al., IEEE EDL 2007, vol28, n°3, p.211
C. Dupré et al., IEDM 2008, p749
E. Bernard, VLSI 2008
Veillaritis, IEDM 2007
Kavalieros, VLSI 2006, p50
Pouydebasque, SNW 2007
F.Arnaud, IEDM 2008
G.Bidal, VLSI 2009
X.Chen et al, VLSI 2008
S. Natarajan et al., IEDM 2008
C.H. Diaz et al. , IEDM2008

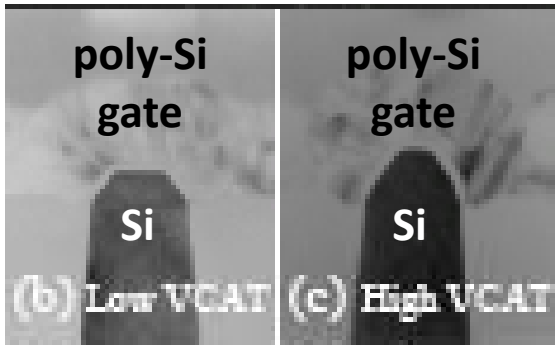
**→ A better solution is needed…**

# The Tri-Gate Bulk FET

M. Kito et al. (Toshiba Corp.), *2005 Symp. VLSI Technology*

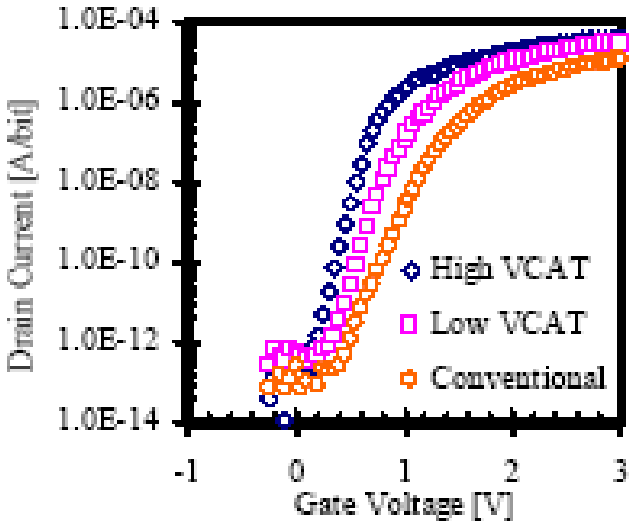
- **A tri-gate structure is easily achieved by slightly recessing the isolation oxide (or by selective epitaxial growth) just prior to gate-stack formation**

**XTEM images**




- **Superior electrostatic integrity is achieved with the tri-gate structure**
  - **→reduced impact of process-induced variations**
  - **→facilitates voltage scaling**

**Measured *I-V* Characteristics**



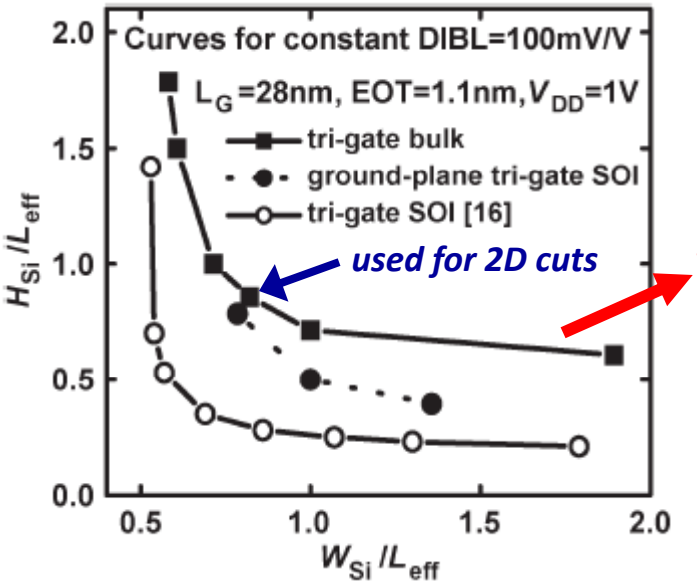
# Outline

- Introduction
- **Tri-Gate Bulk/PD-SOI FET Design**
- Corrugated Substrate Technology
- Summary

# Bulk *vs.* SOI Tri-Gate FET Design

X. Sun *et al.*, *IEEE Electron Device Letters* Vol. 29, pp. 491-493, May 2008.

## Required Si Channel Dimensions

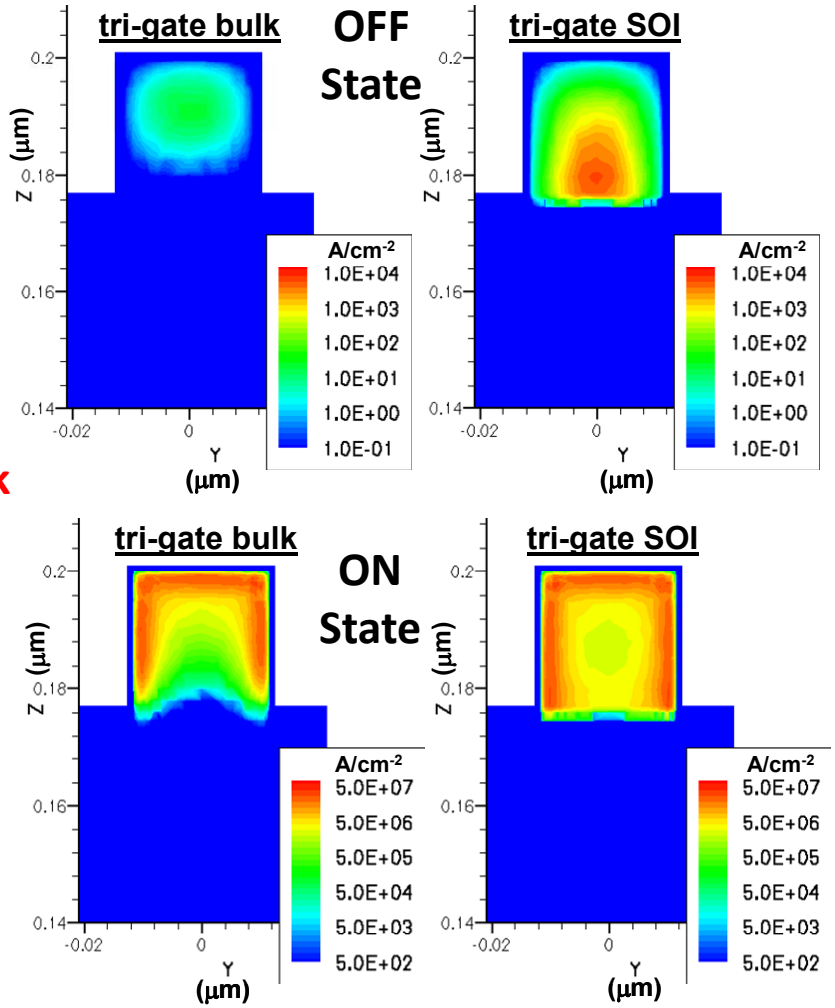



[16] J.G. Fossum *et al.*, *IEDM Tech. Dig.*, pp. 613-616, 2004.

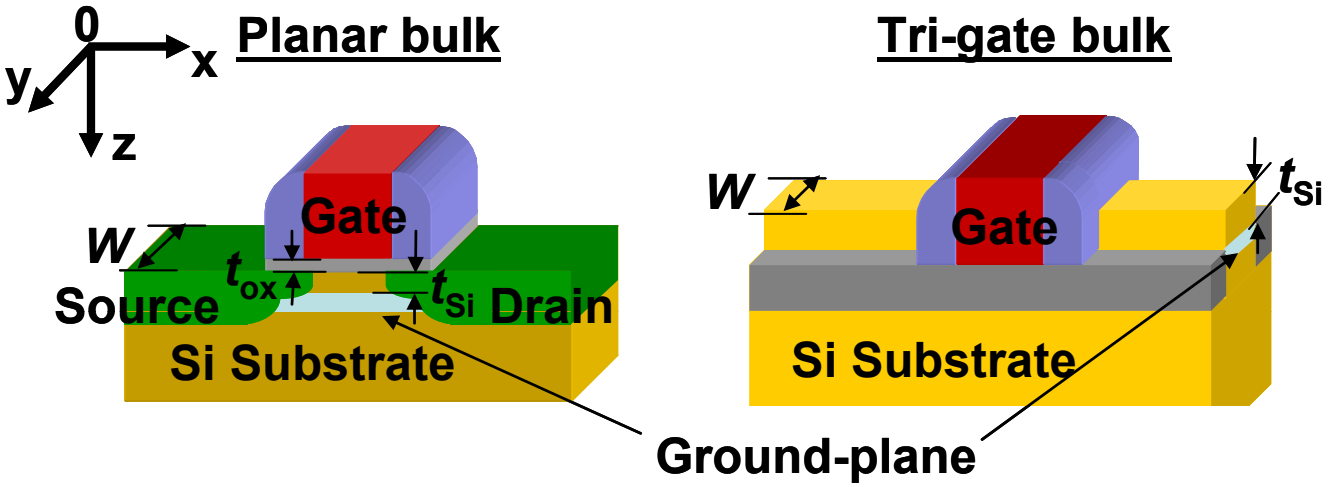
**Wider/taller stripes can be used with bulk design**

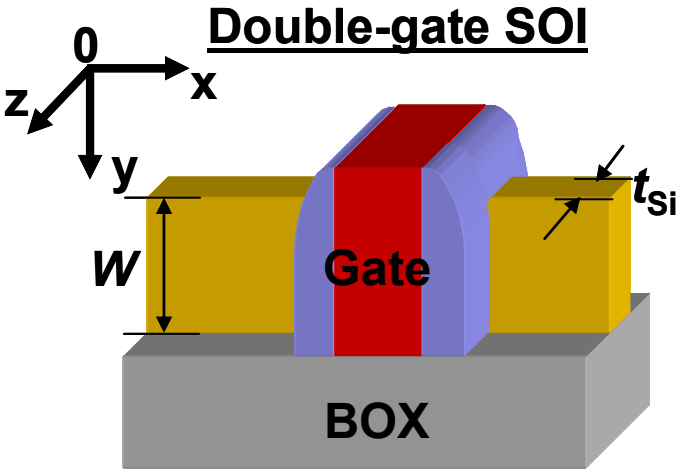
**→ Bulk design achieves better layout efficiency**

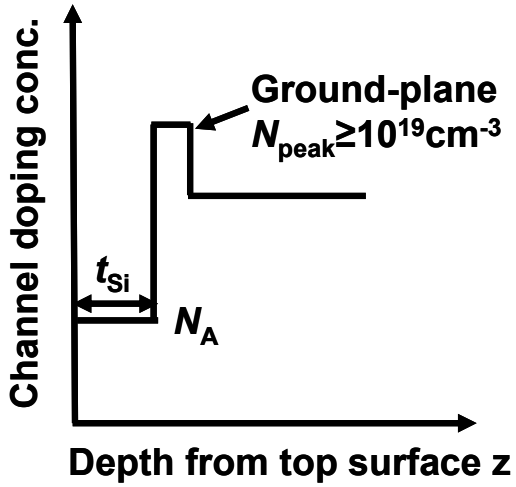
## Current Contour Plots



# Idealized MOSFET Designs



# Tri-Gate Bulk FET: Scale Length Derivation

X. Sun *et al.*, to appear in *IEEE Trans. Electron Devices*

**Poisson's equation:** $\frac{d^2\Phi}{dx^2}+\frac{d^2\Phi}{dy^2}+\frac{d^2\Phi}{dz^2}=\frac{qN_A}{\varepsilon_{Si}}$

**+**

**parabolic potential approximations**

**+**

**appropriate boundary conditions** ⇒ $\frac{d^2\phi(x)}{dx^2}-\frac{\phi(x)}{\lambda^2}=0$

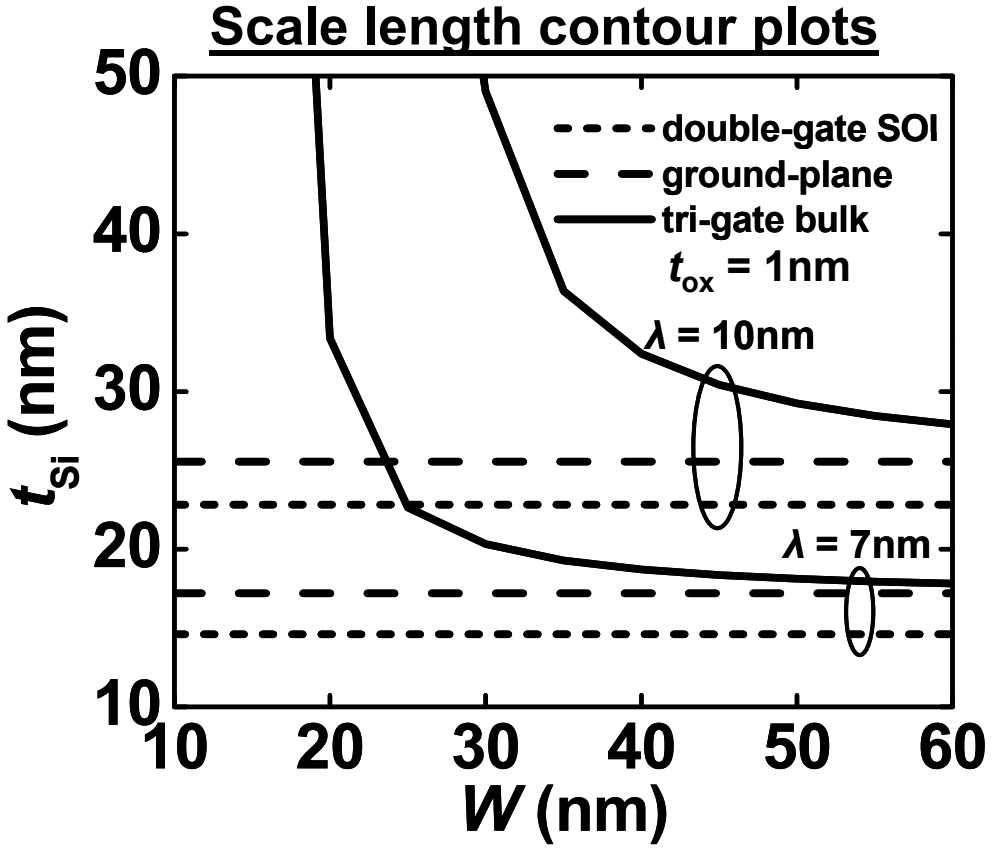
**where $\lambda$ is the scale length:**

$$\lambda=\sqrt{\frac{1+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{z_{leak}}{t_{ox}}-\frac{z_{leak}^2}{t_{Si}^2}-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{z_{leak}^2}{t_{ox}t_{Si}}}{\frac{8}{W^2}\left(\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{z_{leak}}{t_{ox}}-\frac{z_{leak}^2}{t_{Si}^2}-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{z_{leak}^2}{t_{ox}t_{Si}}\right)+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{2}{t_{ox}t_{Si}}+\frac{2}{t_{Si}^2}}}$$

where $z_{leak}=\frac{1}{\frac{2\varepsilon_{Si}}{\varepsilon_{ox}}\frac{t_{ox}}{t_{Si}^2}+\frac{2}{t_{Si}}}$ is the location of the highest leakage current density

# Scale Length Comparison

## Tri-Gate Bulk FET *vs.* Planar Bulk FET *vs.* FinFET

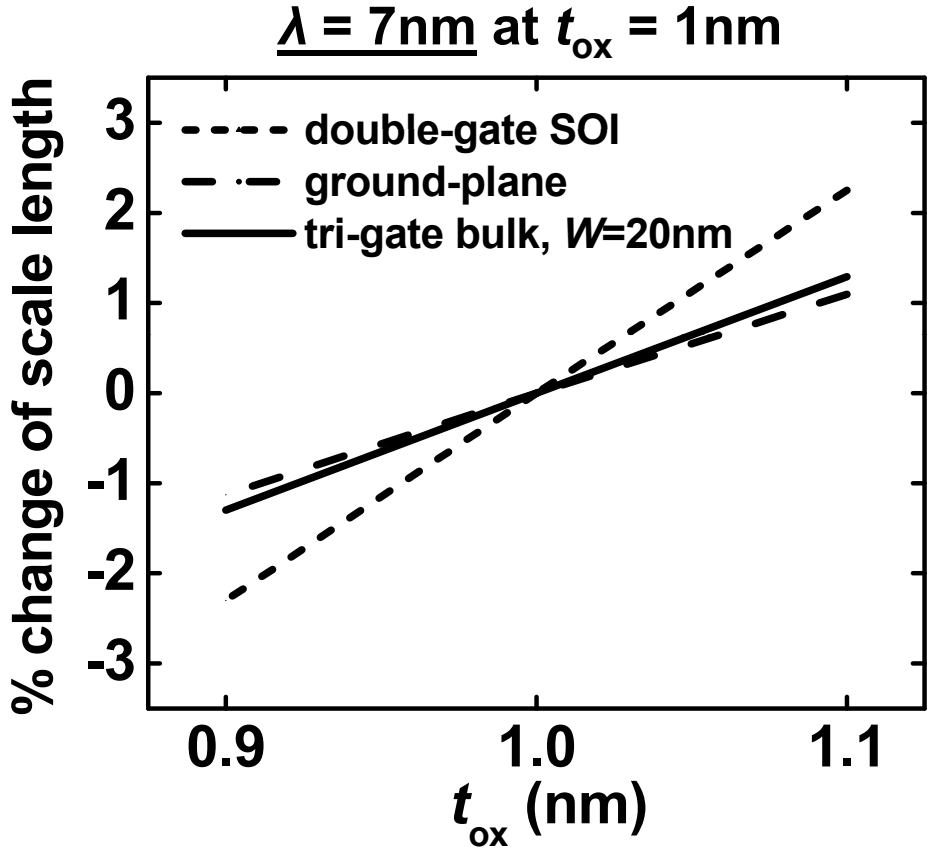



- For given values of $W$ and $t_{Si}$, the scale length is smallest for the tri-gate bulk FET design.

X. Sun *et al.*, to appear in *IEEE Trans. Electron Devices*

# Sensitivity to $t_{ox}$ Variations

X. Sun *et al.*, to appear in *IEEE Trans. Electron Devices*



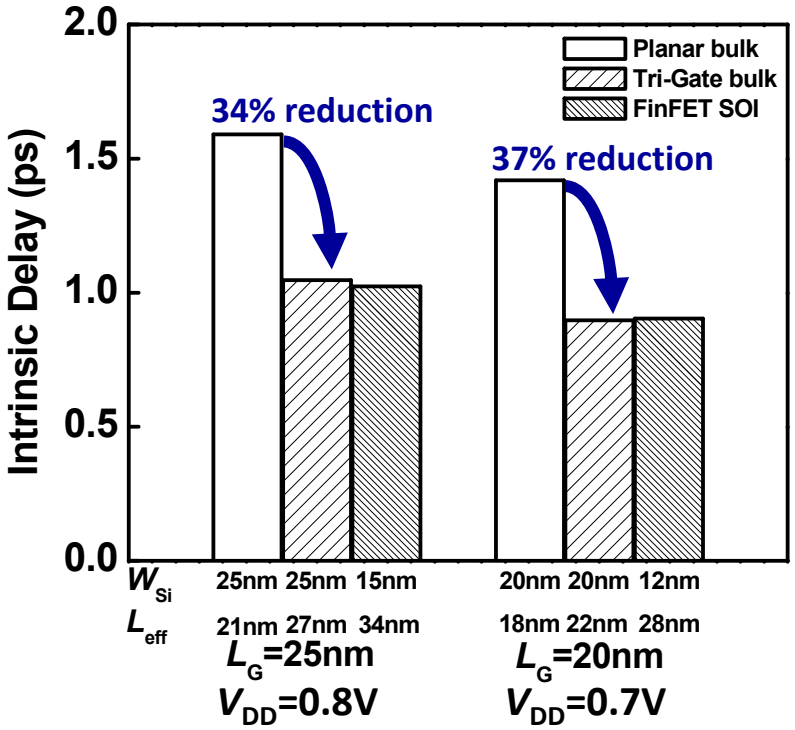

- Tri-gate and planar ground-plane bulk FETs are less sensitive to $t_{ox}$ variation as compared with the FinFET.

# Tri-Gate Bulk FET Advantages

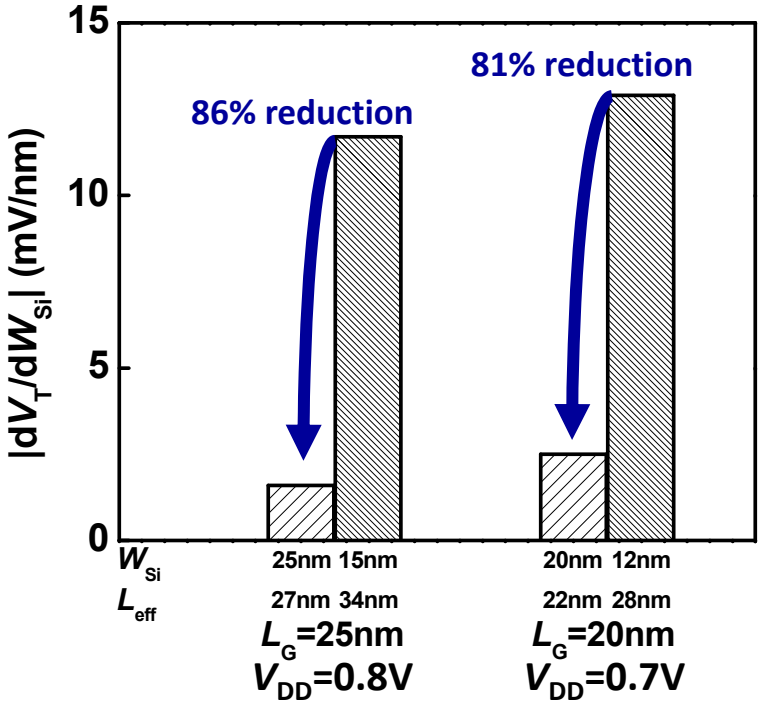
X. Sun *et al.*, to be published

- **3-D device simulations of transistors designed for minimum intrinsic delay for a given off-state leakage specification:**
  - $L_g$=25nm (EOT=1nm): $I_{OFF}$=8nA/μm; $L_g$=20nm (EOT=0.9nm): $I_{OFF}$=18nA/μm

✓ **The delay advantage of the tri-gate bulk FET increases with scaling.**



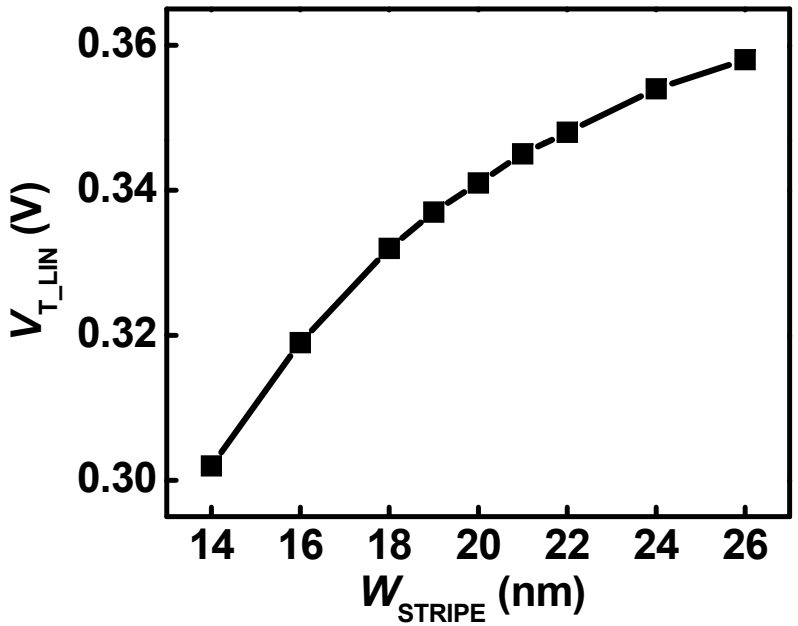

✓ **The tri-gate bulk FET is less sensitive to $W_{STRIPE}$ variation than the FinFET.**



# Impact of $W_{STRIPE}$ Variations

X. Sun *et al.*, to be published

$L_g$ = 20nm, EOT = 0.9nm, $H_{STRIPE}$ = $t_{Si}$ = $X_J$ = 14nm

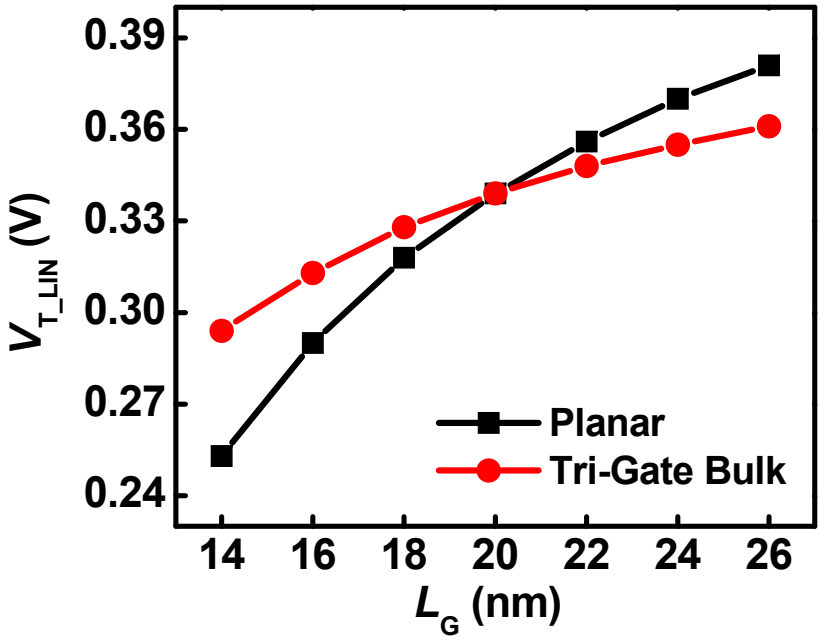



- Smaller $W_{STRIPE}$ → stronger gate control → smaller $V_{TH}$
  - $\Delta V_{TH}$ < 10mV for 10% variation in $W_{STRIPE}$

# Impact of Gate-Length Variations

X. Sun *et al.*, to be published

EOT = 0.9nm, $W_{STRIPE}$ = 20nm, $H_{STRIPE}$ = 7nm, $t_{Si}$ = 14nm, $X_J$ = 7nm




(Channel- and source/drain-doping profiles are identical for the planar and tri-gate MOSFETs)

- The tri-gate bulk FET is less sensitive to gate-length variations, due to improved gate control.
  - Benefit is equivalent to >6Å reduction in $t_{ox}$

# Impact of Gate Line-Edge Roughness

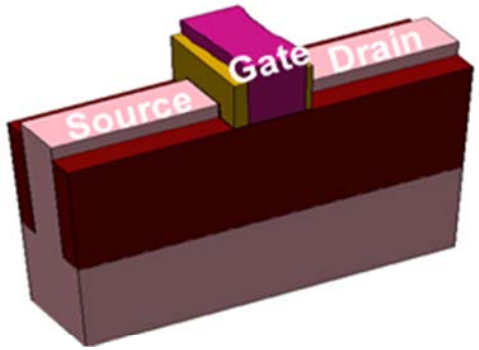
## 3-D Device Simulation Study

**Sample measured LER data using MATLAB code (200 cases)** → **3D Structure Generation** → **Device Simulation**

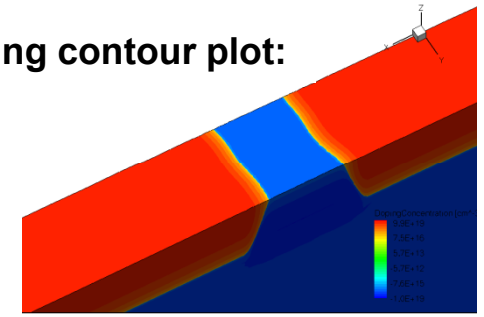
- **Use MATLAB to process LER data to be inputted into Sentaurus Structure Editor**
  → **Perform 3-D device simulation using Sentaurus Device**

- **Assumption**:
  – LWR in $L_{eff}$ is the same as that for the gate electrode.
  (worst case scenario, relevant for ultra-shallow junction technology)

**Tri-gate bulk FET with gate LER:**




**Doping contour plot:**



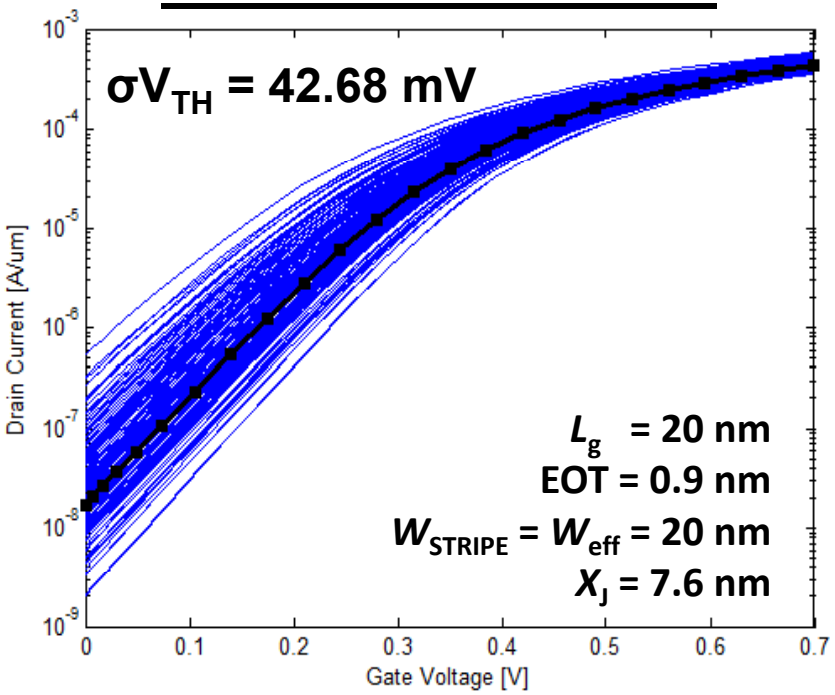
# Simulated $I_D$-$V_G$ Characteristics

X. Sun *et al.*, to be published

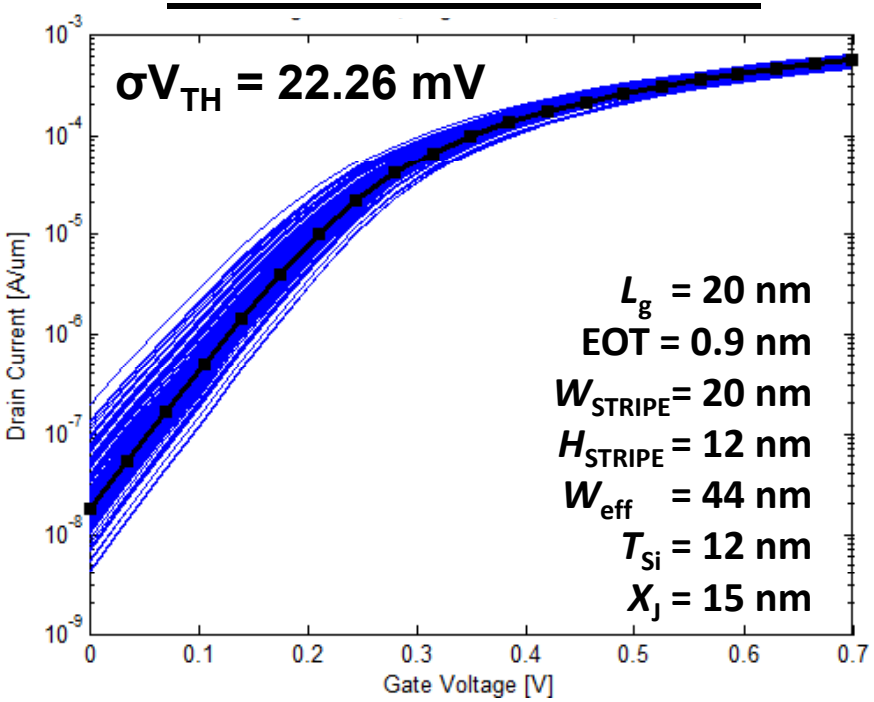
- 200 gate-LER cases were simulated for each structure.
- $I_D$-$V_G$ curves for a nominal structure (without gate LER) are shown in black.

$V_{DD}$ = 0.7 V

**Planar Bulk MOSFETs**




**Tri-Gate Bulk MOSFETs**



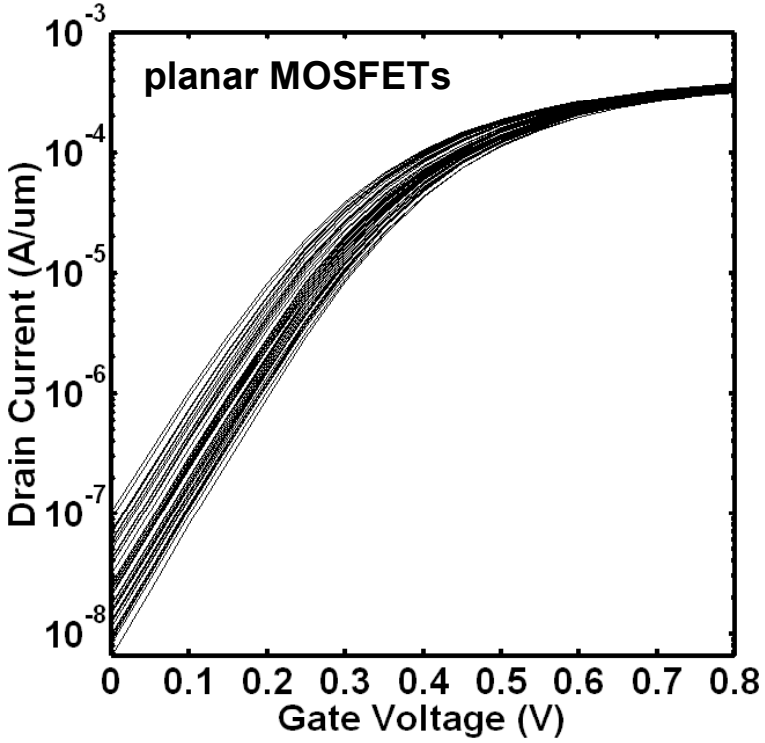
# Impact of Random Dopant Fluctuations

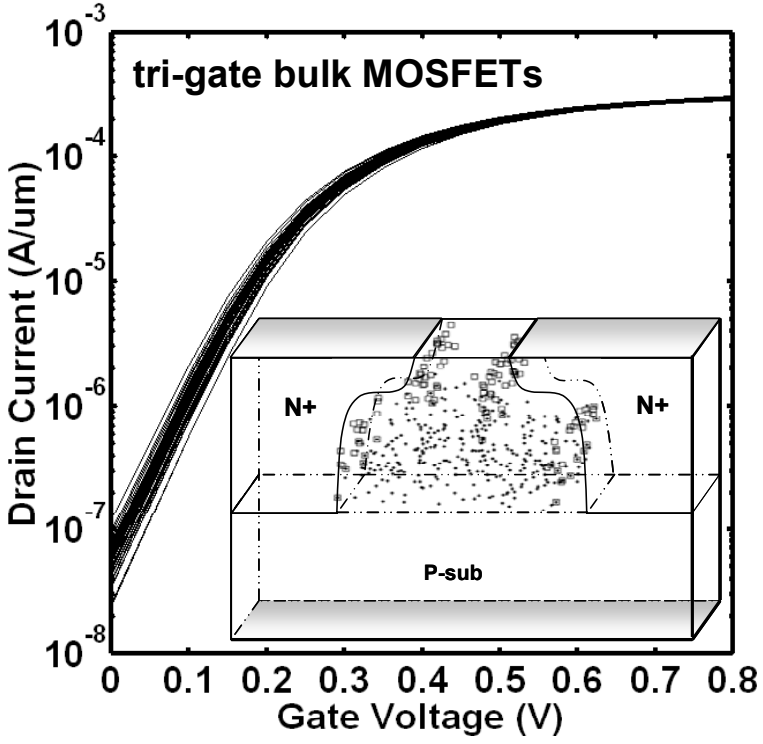
X. Sun *et al.*, *IEEE Electron Device Letters* Vol. 29, pp. 491-493, May 2008.

**Monte Carlo simulations, 100 cases each**

**$L_g$ = 20nm, EOT = 0.9nm, $W_{STRIPE}$ = 20nm, $H_{STRIPE}$ = 14nm, $t_{Si}$ = 14nm, $X_J$ = 14nm**

**$V_{DD}$ = 0.8 V**



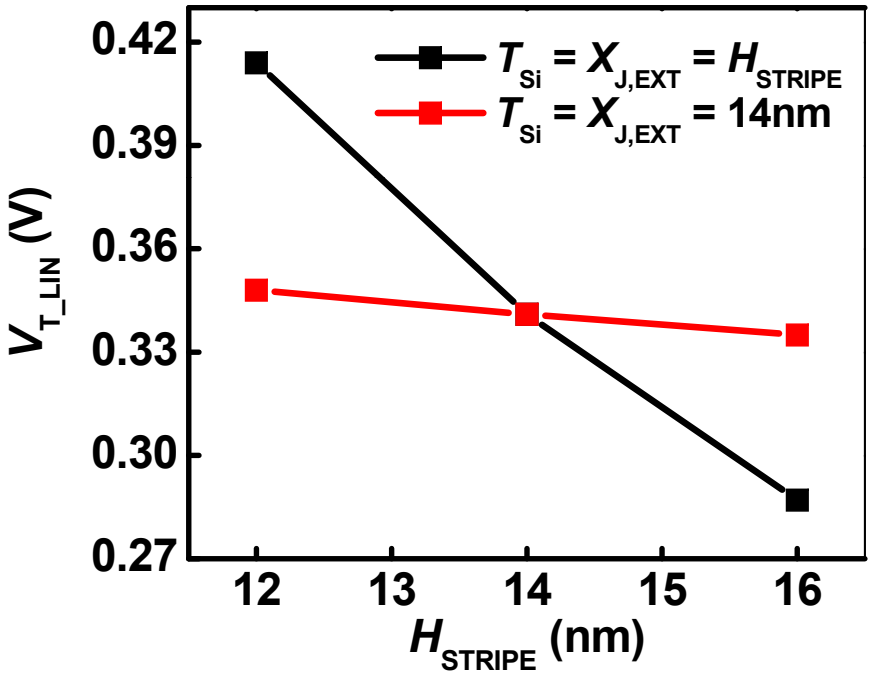




- **The tri-gate bulk MOSFET is less sensitive to RDF effects.**

# Impact of $H_{STRIPE}$ Variations

X. Sun *et al.*, to be published

$L_G$ = 20nm, EOT = 0.9nm, $W_{STRIPE}$ = 20nm

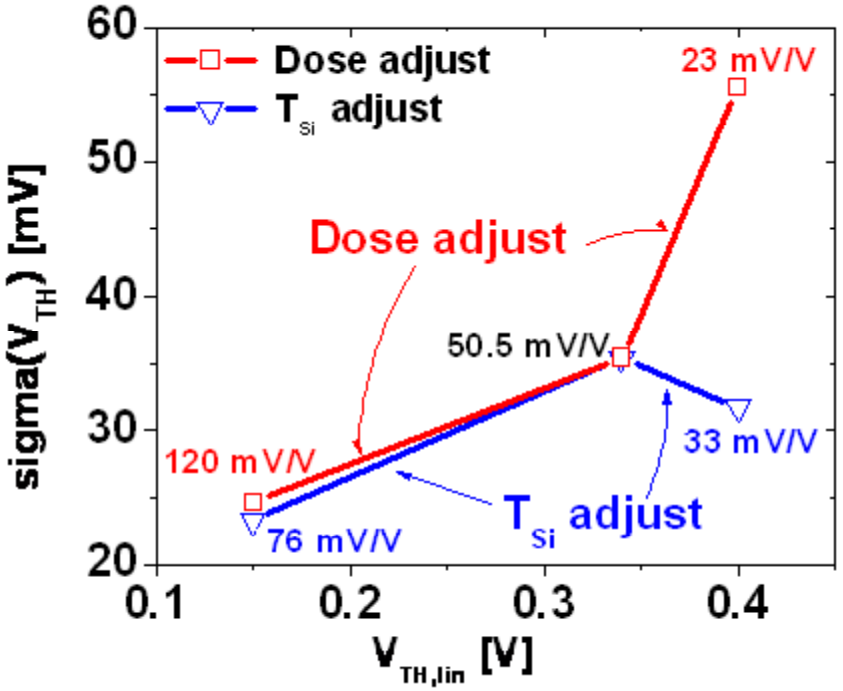



- If $t_{Si}$ is fixed, $V_{TH}$ is not sensitive to $H_{STRIPE}$ variation.

# $V_{TH}$ Adjustment Approaches

C. Shin *et al.*, *IEEE 2008 Silicon Nanoelectronics Workshop*

- $V_{TH}$ of a tri-gate bulk MOSFET can be adjusted by tuning either the dose ($N_{peak}$) or the depth ($t_{Si}$) of the retrograde doping profile.
  - 200 atomistic simulations were run for each nominal design.
- $V_{TH}$ adjustment via $t_{Si}$ tuning provides for less variation, and eliminates the trade-off with short-channel control.



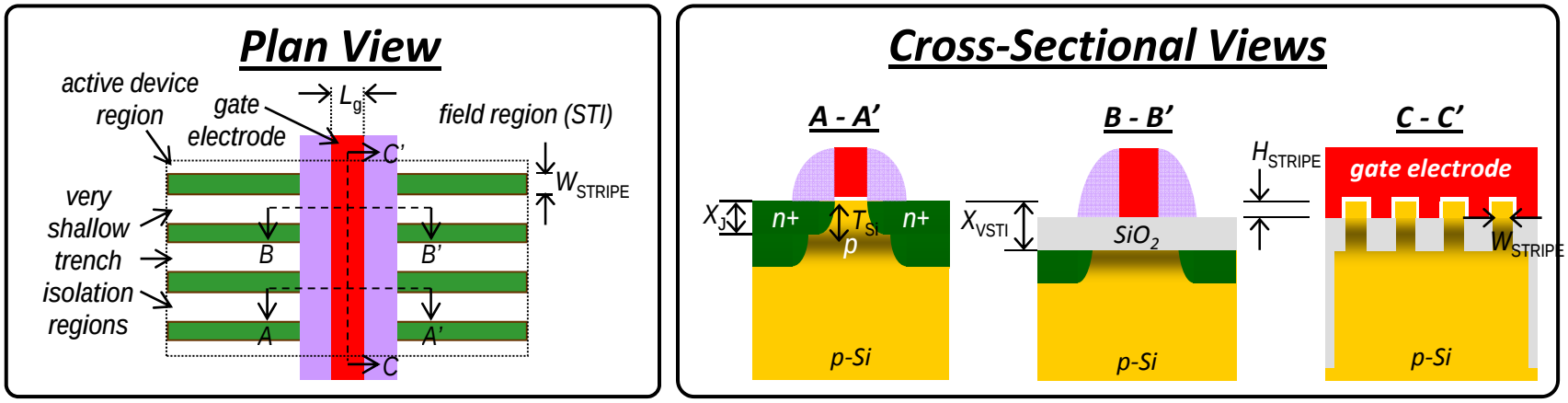

DIBL values for each design are indicated

# Outline

- Introduction
- Tri-Gate Bulk/PD-SOI FET Design
- **Corrugated Substrate Technology**
  - **SegFET fabrication process**
  - **SRAM performance benefits**
  - **Advanced channel materials**
- Summary

# Segmented Bulk MOSFET (SegFET)

- The channel is digitized into stripes of equal width, isolated by very shallow trench isolation (VSTI) oxide
  - The effective channel width is adjusted by adjusting the number of stripes.
  - Each stripe is a tri-gate bulk MOSFET.
- Note that the source/drain regions are contiguous.

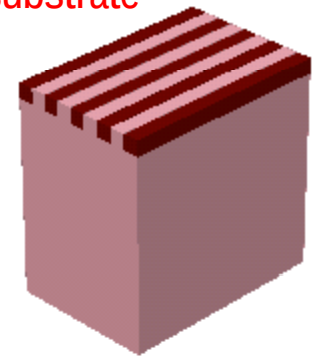



T.-J. King Liu and L. Chang, "Transistor Scaling to the Limit," in *Into the Nano Era*, H. Huff ed. (Springer), 2008.

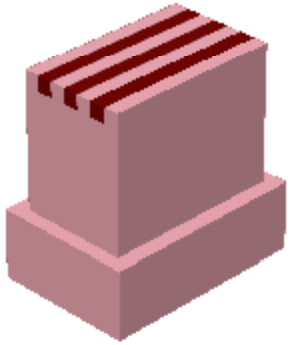
# SegFET Fabrication Process

**T.-J. King and V. Moroz, U.S. Patent 7,265,008**

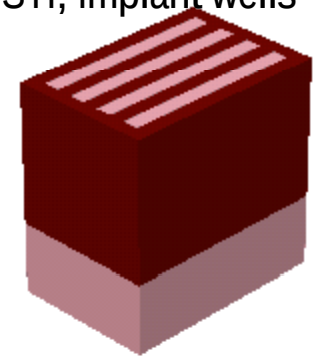
1. Start with corrugated substrate



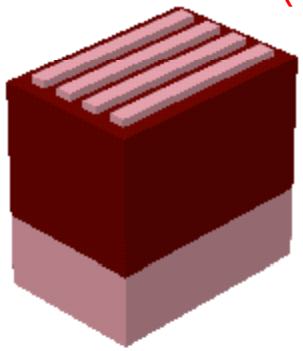
2. Define active areas



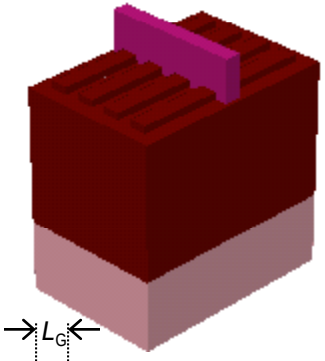
3. Fill trenches to form STI; Implant wells



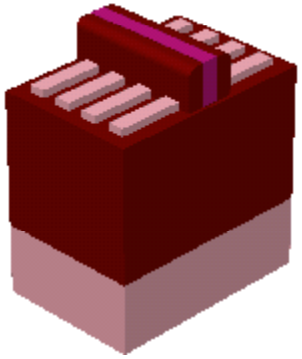
4. Slightly recess the isolation oxide (optional)



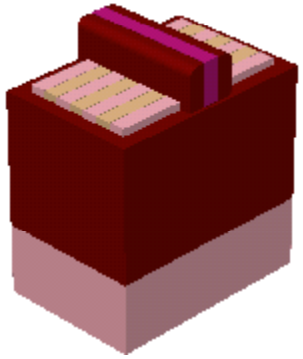
5. Implant channels; Form gate stack



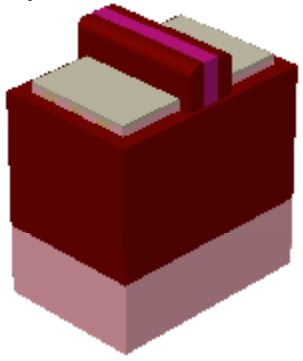
6. Form S/D extensions, then sidewall spacers

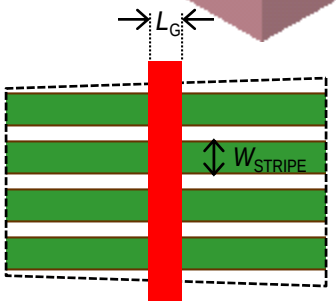


7. Grow epitaxial material in S/D regions (optional)



8. Dope S/D regions; Form silicide



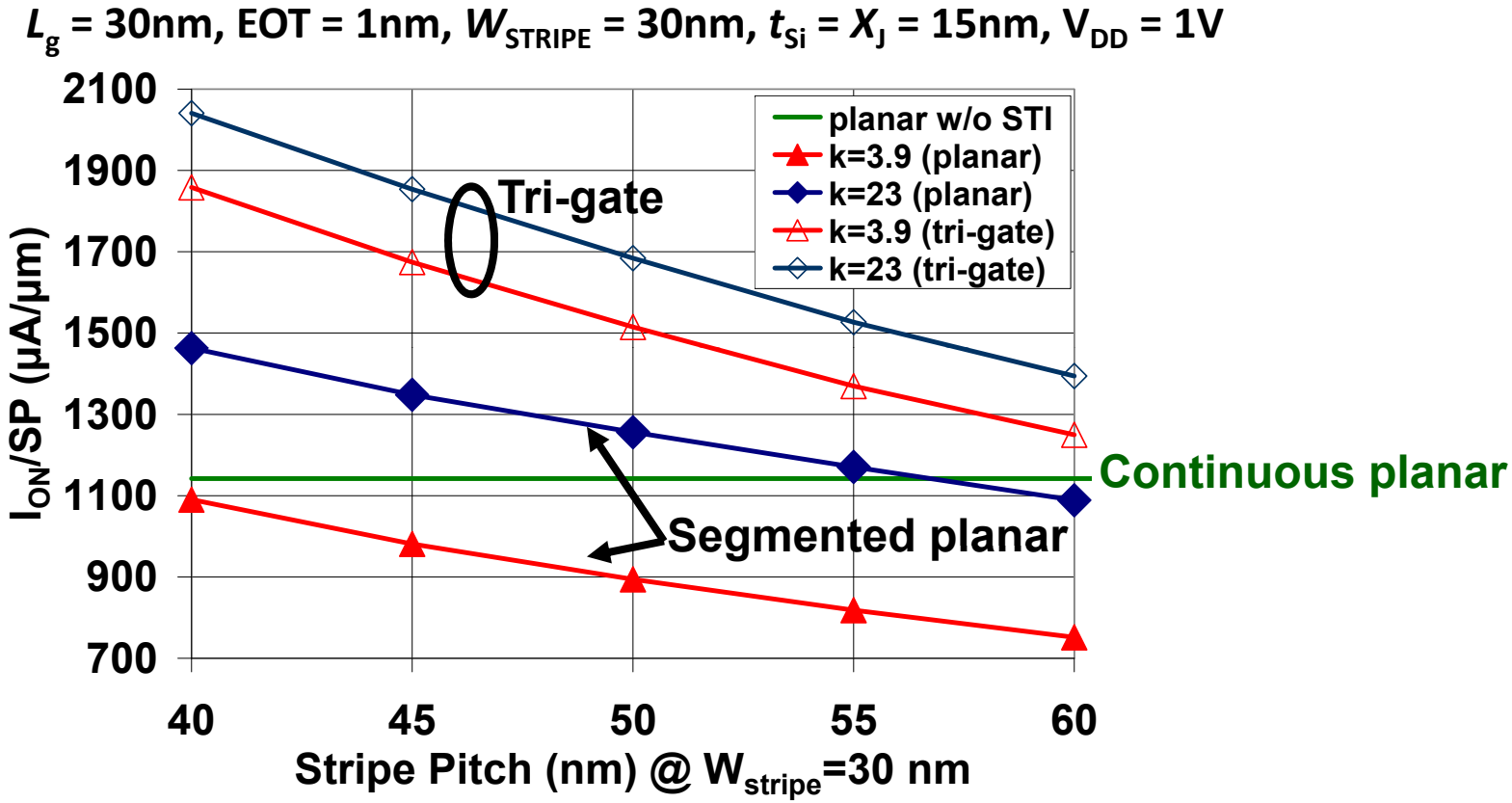



- **Precise control of channel width is achieved.**
  (Layout dependencies and sensitivity to misalignment are reduced.)

→ **reduced variation in MOSFET performance**

# Layout Area Efficiency Comparison

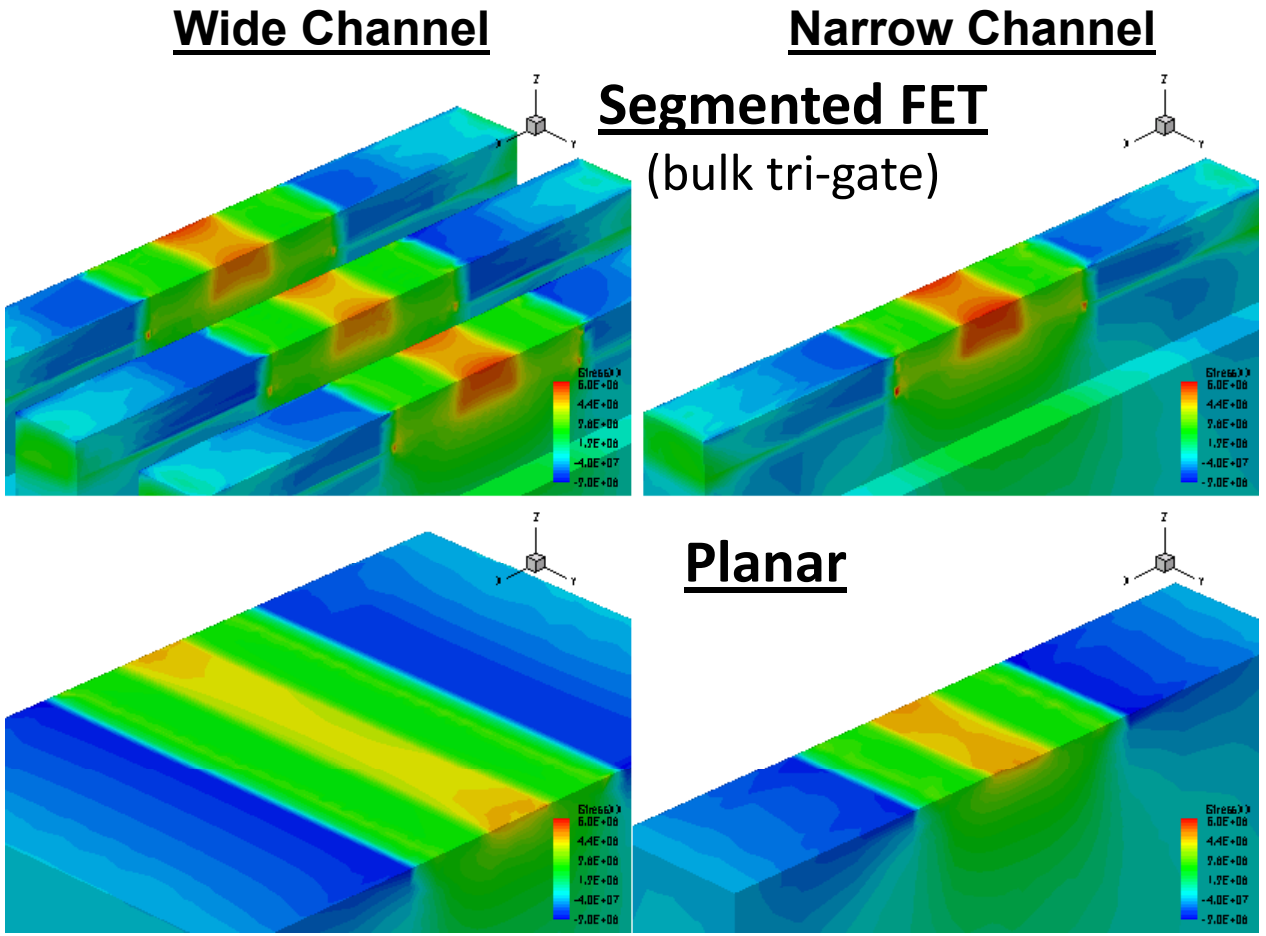
## High-Performance Design




- A segmented planar FET can achieve layout efficiency comparable to that of a conventional planar FET, if $W_{VSTI}$ is very small (<10 nm) or if a high-k dielectric is used as the VSTI material.
- The tri-gate FET achieves superior layout efficiency.

# Impact of Channel Width on Strain Profile

## Capping-layer-induced strain along the channel




Contact etch stop liner is assumed to be a 30nm-thick silicon nitride with 2GPa tensile stress

- SegFET parameters:
  $W_{STRIPE}$ = 20nm
  $W_{SPACING}$ = 20nm
  $H_{STRIPE}$ = 10nm

- $L_G$ = 20nm
- EOT = 0.9nm
- $T_{GATE}$ = 40nm
- $L_{SPACER}$ = 20nm

- **More stress is induced in SegFET → More mobility enhancement**
- **Reduced variation with $W_{eff}$ for SegFET → Reduced $\mu$ variation**

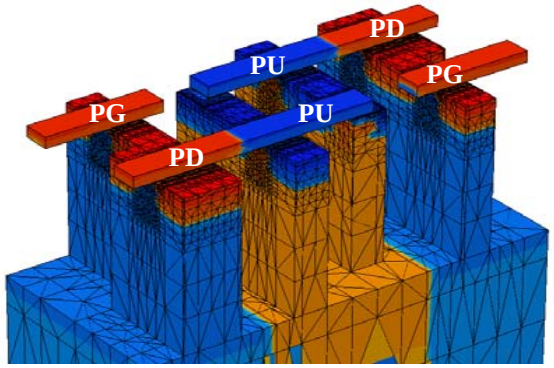
**X. Sun *et al.*, to be published**

# 6-T SRAM Cell Design

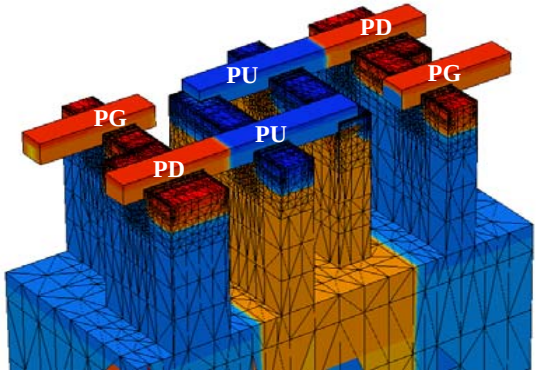
C. Shin *et al.*, presented at the *2009 SISPAD*

- **6-T SRAM cells with comparable α and β ratios were designed, based on 22nm CMOS technology design rules.**
  - **For the SegFET SRAM cell: $W_{STRIPE}$ = 20nm, $W_{SPACING}$ = 15nm**
  - **$W_{SPACER}$ = 15nm (limited by gate-to-contact pitch), $X_J$ ~ 10nm**

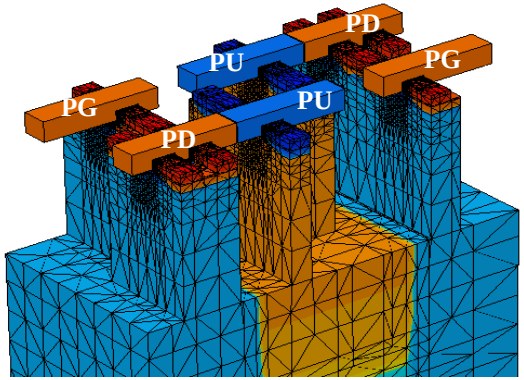
**Simulated Planar SRAM Cell**
(isolation oxide not shown for clarity)




**Simulated Tri-gate bulk SRAM Cell**
(isolation oxide not shown for clarity)




**Simulated SegFET SRAM Cell**
(isolation oxide not shown for clarity)

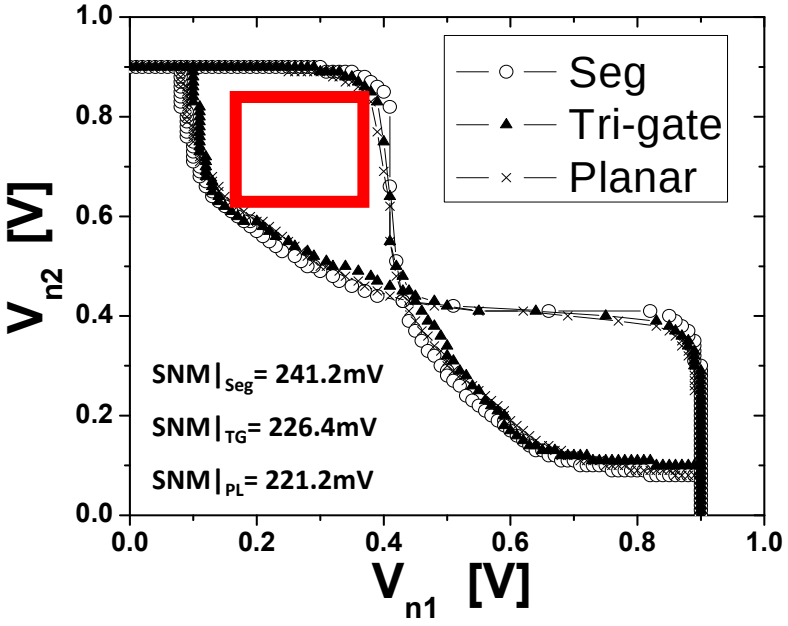


# Simulated Read and Write Margins

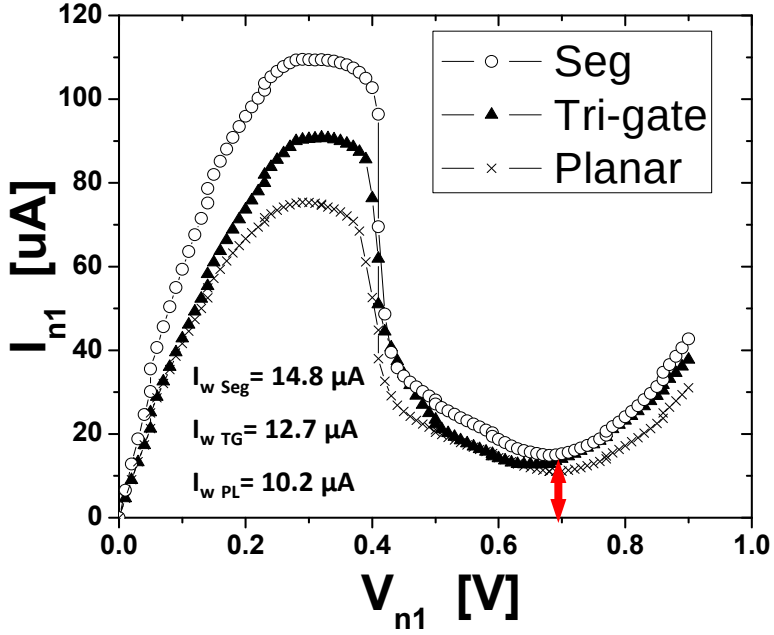
C. Shin *et al.*, presented at the *2009 SISPAD*

- **SNM is largest for the SegFET cell: 241 mV *vs.* 221mV for the planar bulk MOSFET cell**
- **$I_w$ for the SegFET cell is also superior to that for the planar bulk MOSFET cell.**

**Butterfly curves**




**Write-N-curves**

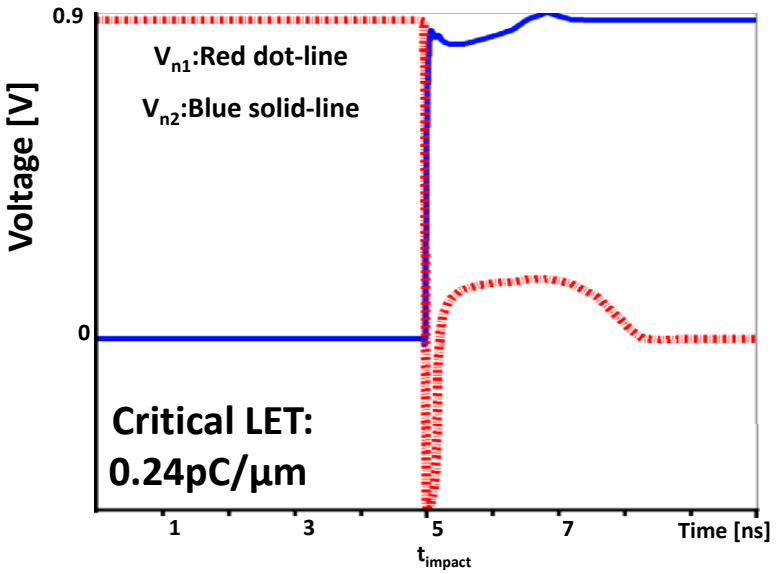


# Single-Event-Upset Comparison

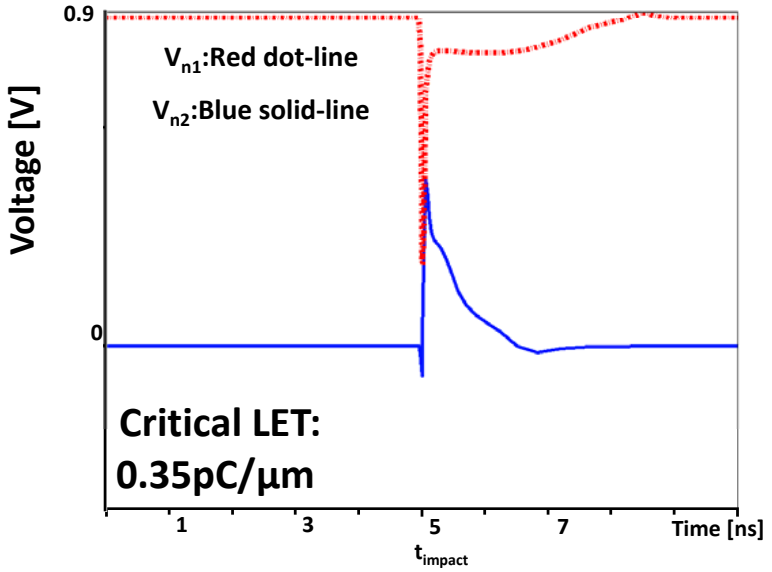
## Full 3-D transient simulations

- When a heavy-ion beam impinges on the high ("1") storage node at time $t = t_{impact}$, the generated $e^-/h^+$ can turn on a parasitic thyristor, shorting the drain node to the source node.
- The SegFET cell is more robust to a given ion-beam strike.
  - Possible explanations: stronger pull-up device, slightly larger internal capacitance, or smaller body effect.

**Planar MOSFET SRAM Cell**




**SegFET SRAM Cell**




C. Shin *et al.*, presented at the *2009 SISPAD*

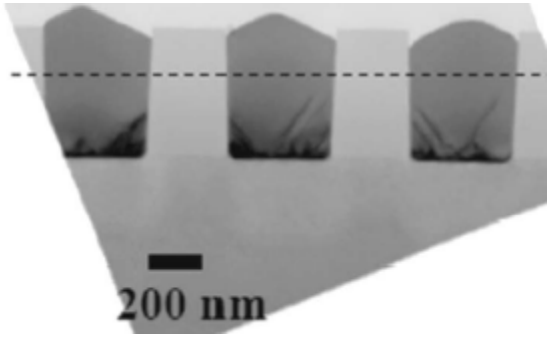
# Advanced Channel Materials

- **High-mobility semiconductor materials can potentially provide for improved performance:**
  - Ge for PMOS
  - (In)GaAs for NMOS

| | Si | Ge | GaAs |
|---|---|---|---|
| **Electron mobility** ($cm^2/Vs$) | 1500 | 3900 | 8500 |
| **Hole mobility** ($cm^2/Vs$) | 450 | 1900 | 400 |
| **Lattice constant** (Å) | 5.431 | 5.646 | 5.653 |
| **Band gap** (eV) | 1.12 | 0.66 | 1.424 |
| **Dielectric constant** | 12 | 16 | 13 |

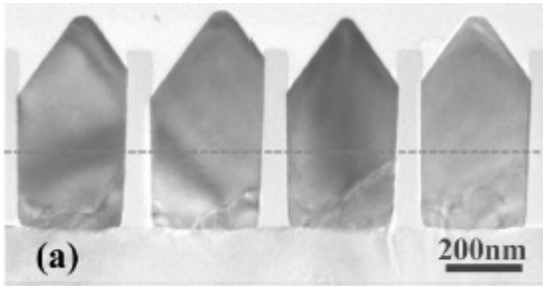
- **Selective epitaxial growth directly on Si is facilitated by the use of a corrugated substrate:**

**Ge on Si**




J.-S. Park *et al.*, *Appl. Phys. Lett.* 90 052113, 2007

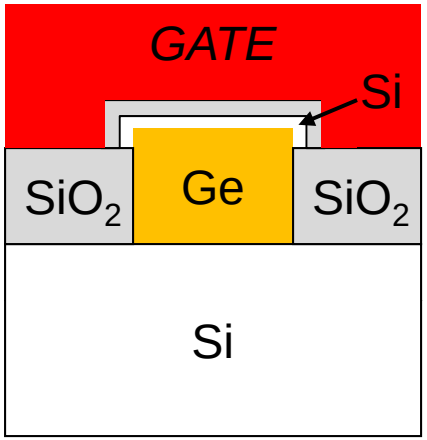
**GaAs on Si**



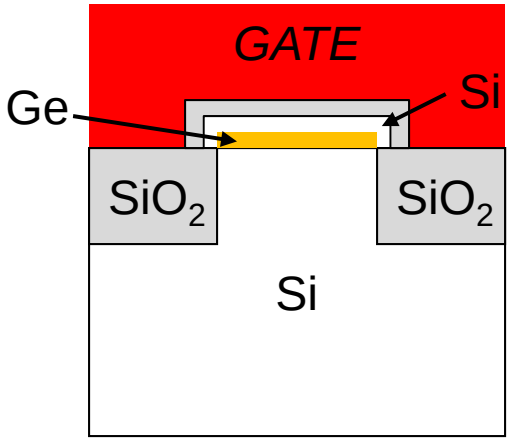

J. Z. Li *et al.*, *Appl. Phys. Lett.* 91 021114, 2007

# Ge Integration Options

- **Homogeneous semiconductor stripes:**
  - Relaxed (unstrained) channel
  - High BTBT leakage due to small $E_g$
  - Significant DIBL due to large $\varepsilon_r$




- **Heterogeneous semiconductor stripes:**
  - Thin, strained channel
  - Reduced BTBT leakage
  - Reduced DIBL



# Outline

- Introduction
- Tri-Gate Bulk/PD-SOI FET Design
- Corrugated Substrate Technology
- **Summary**

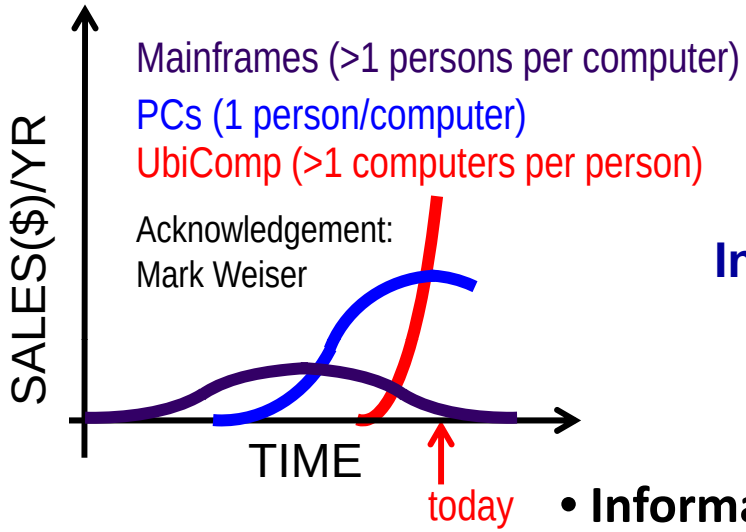
# Summary

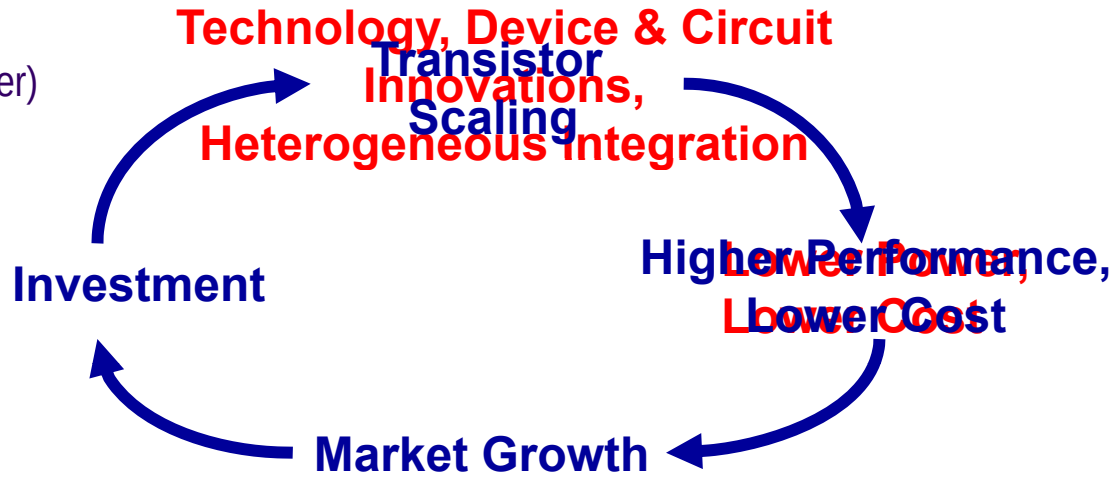
- **Power density and variability now limit transistor scaling**
  - **Known (ITRS) solutions are *revolutionary* and therefore costly**
- **Tri-gate bulk MOSFET (corrugated substrate) technology offers an *evolutionary* (low-cost) pathway to lower $V_{DD}$, reduce $V_{TH}$ variability, and extend transistor scaling**
  - **utilizes conventional (established) IC fabrication techniques**
  - **is compatible with technologies developed to date (*e.g.* metal-gate/high-k dielectric, strained-Si) for bulk/PD-SOI CMOS**

**… that is almost transparent to end users**

- **Established compact models; zero design cycle time impact**
- **Minimal (non-disruptive) impact on design style**

# The Age of Ubiquitous Computing

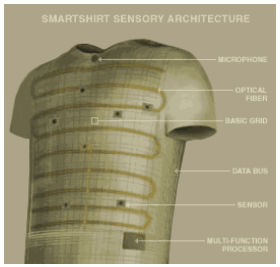



- **Information technology for better quality-of-life**
  - **pervasive**
  - **embedded**
  - **human-centered**
  - **solving societal-scale problems**

Philips

Sensatex




Transportation

Energy

**$370 Billion**
Total U.S. Annual Energy Costs

Environment

**200%**
Increase in U.S. Electricity Consumption since 1990

**40%**
Total U.S. Energy Consumption for Buildings

Health care

Disaster response

**72%**
Total U.S. Electricity Consumption for Buildings

**55%**
Total U.S. Natural Gas Consumption for Buildings

# Acknowledgements


- **FLCC & IMPACT project corporate sponsors**
- **UC Discovery Grants Program**
- **Semiconductor Research Corporation**