Advanced Substrates for CMOS

Nathan Cheung
Dept of EECS, UC-Berkeley
cheung@eecs.berkeley.edu
OUTLINE

• Motivations for UT-SOI, SSOI, and GeOI

• Substrate Fabrication Methods and Manufacturing Issues

• Compatibility with CMOS device structures
Ultra-thin SOI MOSFET

• Advantages
  – Extension of existing architecture
  – Si thickness can be used to control the short-channel effects
  – Low Junction Capacitance
  – Steeper subthreshold slope

• New Source/Drain Challenges:
  – Silicide fully consumes the ultra-thin Si layer
  – Large contact resistance
  – High leakage

• Elevated source/drain is required
  – Epitaxy on ultra-thin silicon
  – Thermal Instability is a concern
Why Strained Si?

65 nm transistors exhibit 10-15% increase in drive current with enhanced strain.

INTEL - August 2004
Local Strain Management

*Traditional Approach*
- Graded SiGe Layer
- Biaxial Tensile Strain

*This Technology*
- Selective SiGe S-D
- Uniaxial Compressive Strain
- Tensile Si₃N₄ Cap
- Uniaxial Tensile Strain
Local Stress Management

Figure 2. Cross-sectional secondary electron microscope images of strained Si transistors fabricated in partnership with AmberWave Systems: (a) 90nm gate length strained Si transistor fabricated at UMC and (b) 25nm gate length strained Si transistor fabricated at AMD.
Desired Types of Uniaxial Stress

Desired Stress:

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<tr>
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<th>Tran.</th>
<th>Long.</th>
<th>Z</th>
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<tr>
<td>pFET</td>
<td>T</td>
<td>C</td>
<td>T</td>
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<tr>
<td>nFET</td>
<td>T</td>
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T: Tensile stress
C: Compressive stress
Motivations of Ge as Material Channel

For channel length in the range of ballistic transport:

• Initial velocity ("low field mobility") is more important than saturation velocity

• Lower contact resistance with smaller barrier Schottky junctions

• Non-SiO2 high-K dielectric will be used anyway
Direct Layer Transfer of 1% Strained Si on Si

Preferential etch of misfit dislocation

Issaacson et al., JECS, 2006
Heteroepitaxial Growth of Ge on Si

With H₂ anneal dislocations are confined to the Si/Ge interface leaving defect free top Ge layers.

Nayfeh, Chui, Yonehara and Saraswat, MRS 2005 Spring Meeting, San Francisco
Wafer-Scale Layer Transfer Approach

Splitting By Internal Force

Donor wafer
H peak
SiO2
Handle wafer

H^+

Wafer bonding

Thermal exfoliation > 400°C


Splitting By External Force

Mechanically weakened Layer

Donor wafer

SiO2
Handle wafer

Wafer bonding

Edge initiated crack propagation

Yonehara et al, *APL*, 64, 2104 (1994)
Strained Silicon Directly on Insulator

- Similar to Ultra-thin SOI
- Enhanced Mobility
- Strained Silicon w/o SiGe
  - *Ge diffusion into Si is not an issue*
  - *Integration is simpler*

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**I**  
Si Epi on SiGe Buffer

**II**  
Oxide Growth + Dep

**III**  
Hydrogen Implantation

**IV**  
Bond Si Wafer

**V**  
Smart Cut

**VI**  
Etch SiGe
Buffered SiGe layer cannot be too thin

Figure 1. Cross-sectional transmission electron microscope images of (a) entire strained Si substrate structure with (b) close-up of strained silicon device film

Source: AmberWave Systems
Characteristics of Strained-Si SOI wafer

Thickness

10-20 nm for Fully Depleted devices *

70 nm for Partially Depleted devices

Stress values are 1.5 GPa ± 20 MPa, 1σ variation.

*Critical thickness is ≤20 nm for the silicon layer thickness when grown on a 20% SiGe relaxed layer at an 800°C corresponding growth temperature.
Strain Stability with thermal annealing

Raman shift represents a strain of about 1.2 GPa

Thermal stability for a 20 nm sSOI layer after heat treatment for 30 minutes

Source: Soitec/ASM
Uniaxial Strain SSOI

- Modify bond and cleave processes
- Prestress Bond Process
  - Bond donor and handle wafers curved
  - Stress is “locked” in depending on respective wafer thicknesses
    - Tensile: Donor convex, Handle concave
    - Compressive: Donor concave, Handle convex
- Cleave Wafers under stress
  - Cleaved film stress further increases due to handle wafer unbending

http://www.sigen.com
Advantages of Wafer-Scale Layer Transfer

- Donor wafer can be recycled
- Transferred thickness and buried oxide thickness are *independently* controlled
- (100), (110), and (111) Epi layers can be transferred
- Multi-stack structures can be transferred

- Embedded enhancements less sensitive to process variability across wafer
- Boosted performance when combined with localized strain and novel device structures.
SOI (Canon)

Strained Si SOI (SiGen)

Strained Si SOI (SOITEC)

Si on Quartz (SiGen)
Manufacturing Issues
Bonding Defects and Particulate Defects

“Pillow” Defects due to Surface residual contamination prior to bonding

Trampoline Defects of SSOI
Manufacturing Issues
CMP is required to reduce deposited film roughness!

Deposited Poly: RMS roughness ~10.2 nm
NOT BONDABLE

After CMP: RMS roughness ~0.93 nm
BONDABLE

Epi SiGe as grown  Epi SiGe after CMP
Manufacturing Issues
Surface Smoothing

As-split surface (SOI)

After-anneal surface

![Graph showing Rrms (nm) vs. L (µm) for As-Etched, H₂ Annealed, and Bulk Wafer surfaces.](image)
SEM of GeOI surface after Mechanical-Cut

AS-M-CUT@220°C GeOI SURFACE

SEM of GeOI surface after CMP

CMP smoothed GeOI surface

• RMS of GeOI surface can be smoothed down by CMP to 0.3nm

Eric Liu, UCB
Manufacturing Issues
Total Thickness Variation with <30nm transfer

Implantation in Si: H+ 175 keV 5.0 x 10^{16} cm^{-2} 600C

*Crack derailing affects transferred layer thickness variation
*Substrate stress affects transferred layer thickness
*Hydrogen gettering by SiGe affects transfer thickness
Mixed-Mode Crack Propagation

Stress intensity factor of the kink crack inclined at $\alpha$ to the main crack

\[
K_1 = c_1 k_1 + c_2 k_{II}
\]
\[
K_{II} = c_3 k_1 + c_4 k_{II}
\]

Where $k_1$ and $k_{II}$ are the stress intensity factors acting on the main crack and,

\[
c_1 = \frac{1}{4} \left( 3 \cos \frac{\alpha}{2} + \cos 3 \frac{\alpha}{2} \right)
\]
\[
c_2 = -\frac{3}{4} \left( \sin \frac{\alpha}{2} + \sin 3 \frac{\alpha}{2} \right)
\]
\[
c_3 = \frac{1}{4} \left( \sin \frac{\alpha}{2} + \sin 3 \frac{\alpha}{2} \right)
\]
\[
c_4 = \frac{1}{4} \left( \cos \frac{\alpha}{2} + 3 \cos 3 \frac{\alpha}{2} \right)
\]

Loryuenyonth et al, UCB
Manufacturing Issues
Epi donor wafer is preferred

• **SOI** Less COP (Crystal Originated Particle) defects than CZ Si wafers

- [Image of COP defects]

• **GeOI** No 300mm Ge bulk wafers yet

• **s-SOI** Strained layer is formed epitaxially on SiGe buffer layers
Double Gate MOSFET

FIGURE 6.2 Generic features of double gate MOSFET device.
Ultra-Thin (<1KÅ tSOI) Non-Uniformity

Range (Max-Min) (Å)

Ultra-Thin SOI Layer Thickness

10%

Early 2002
Late 2002

Typical Range <25Å

Range Now Independent of Layer Thickness

Device Layer Thickness (Å)
FinFET does not require ultra-thin overlayer

- **Self-aligned gates straddle thin silicon fin**
- **Current flows parallel to wafer surface**

![Diagram showing FinFET structure](image)

- **Gate Length** = $L_g$
- **Fin Height** = $H_{fin} = W$
- **Fin Width** $W_{fin} = T_{Si}$
Impact of FinFET Orientation

Source: Professor T-J. King (UCB)

Hole Mobility

Electron Mobility
GeOI Research Issues

Metal-Ge contacts (which metal?)

Interface Charge of bonded interface

(to be investigated)
Optimization of GeOI Substrate

Plasma-Assisted Bonding Strength

The bonding interface charge $< Q_f \sim 10^{11}/\text{cm}^2$, positive

Eric Liu, UCB
Challenges for Advanced Substrates

Price (200mm wafers):
- Epi (p-/p+) ~$80
- SOI ~$200
- sSOI and GeOI ~$200

Strained Si
- Dopant activation and dopant diffusion characteristics are altered if Ge is in the substrate.
- Strain distribution can depend on device structure

GeOI
- New processing recipes from cleaning, doping, etching, to metallization
- High-K dielectric/Ge Interface