Critical Dimension Control and its Implications in IC Performance

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FLCC, 10/23/06
Critical Dimension in Perspective  
(Leff in particular)

• Controls both leakage and saturation current  
• Depends on Litho, Etch, Implant, Diffusion, Annealing  
• Its components can be measured with limited precision:  
  – CD SEM: 1-2nm  
  – Ellipsometry: ~0.5nm  
  – Electrical: ~0.2nm  
• Has “hierarchical” nature with different variation mechanisms  
  – Wafer to wafer  
  – Across wafer  
  – Across field, in 100’s of µm distances  
  – Feature to feature, due to pattern density, etc.  
  – Line edge roughness in 10’s of nm distances  
• Industry strives to keep TOTAL variability under 10%. This means 3 sigma total of less than 1nm in the next couple years.
Outline

• CD Control
• CD Modeling
• IC Performance Impact
• New Directions
Some of the recent advances in CD Control come from added Process Visibility – PEB, for example.

- **Uniformity Control**
- **Transient heating and cooling**

*Courtesy OnWafer Technologies*
PEB Temp Control Using Wireless Metrology using multi-zone plate modeling and feedback

Before

Target = 120°C

2.700°C

After

0.175°C

16 plates, 120 °C Target

Courtesy OnWafer Technologies
Post Exposure bake Driven CDU Improvement

- Optimize Temperature
- Optimize CD
- Across Plate
- Plate to Plate

Process of Record

Courtesy OnWafer Technologies
We can also monitor Plasma Etch Temperature...
Present Status of “Active” CD Control

Exposure
- PA Bake
- Spin
- HMDS
- PD Bake

Etch
- PEB
- Develop

Poly Etch System

Etch
- Etch
- Etch
- Etch

Photoresist Removal
- ADI
- AEI
- ELM
On-wafer and in-line metrology in pattern transfer

Exposure

PA Bake

Bake

Thin Film

Spin

Develop

HMDS

OCD

Etch

Poly Etch System

Etch

Etch

Photoresist Removal

OCD

OCD

ELM

I(x, y)

T(t, x, y)

V(t, x, y)

E(t, x, y)

...

T(t, x, y)

V(t, x, y)

E(t, x, y)

...

T(t, x, y)

V(t, x, y)

E(t, x, y)

...

T(t, x, y)

V(t, x, y)

E(t, x, y)

...

I(x, y)
CDU control has to incorporate many strategies.

- Exposure
  - PA Bake
  - PEB
  - Thin Film FB/FF Control
  - Spin
  - PD Bake
  - HMDS
  - OCD Profile Inversion FB Control

- Etch
  - T (t, x, y)
  - FF control
  - Optimal Pattern Design
  - I (x, y)

- Poly Etch System
  - T (t, x, y)
  - V (t, x, y)
  - E (t, x, y)
  - FF/FB Control, chuck diagnostics

- Photoresist Removal
  - OCD FB/FF Control
  - ELM

- OCD FB Control

BCAM

10/23/2006
Experiments

Various PEB plate parameters determine behavior in each segment. These parameters were varied and CD data was collected at the same time.

Dynamic Profile V.S. CD – 9 factors

- Overshoot mean
- Overshoot range
- Steady state mean
- Steady state range
- Steady state duration
- Heating rate mean
- Heating rate range
- Cooling mean
- Cooling range

- 9 thermal-related factors are extracted and linked to CD maps.
- Regression analysis is performed to establish statistical significance.
Within Lot CDU Summary

4 PHP/4DEV

Baseline
20 Wafers
Across Wafer CDU = 3.8nm
CD range 3.4nm

Adjusted
20 Wafers
CDU = 3.5nm
CD range 1.5nm

2nd iteration
25 Wafers
CDU = 3.5nm
CD range 1.0nm

• Dramatic CDU improvement was achieved with TCM
Supervisory Control with Wireless Metrology

- Across-wafer (AW) CD (gate-length) uniformity impacts IC performance
  - Large AW CDV → large chip-to-chip performance variation
  - low yield

- How to cope with increasing AW CD variation?
  - Employ design tricks, e.g., adaptive body biasing, which has limitations
  - Reduce AW CD variation during manufacturing is the most effective approach
CD Uniformity Control Approach

- Making each process step spatial uniform is prohibitively expensive
- Our approach: manipulate PEB temperature spatial distribution of multi-zone bake plate (and die-to-die dose) to compensate for other systematic across-wafer CD variation sources

CDU Control Framework

Optimizer → CD Metrology

Spin/Coat/PAB → Exposure → PEB → Develop → Etch

Optimal die-to-die dose map
Optimal Spatial PEB distribution
Multi-zone PEB Bake Plate

Approximate schematic setup of multi-zone bake plate

Each zone is given an individual steady state target temperature, by adjusting an offset value

\[ T = T_{\text{target}} - \text{Offset} + \text{effect of other zones} \]

Zone offset knobs \[ \Delta O \]

\[ \Delta T(x, y) \Rightarrow \Delta CD(x, y) \]
Develop Inspection (DI) CDU
Control Methodology II

• DI CD is a function of zone offsets

\[
\vec{T} = \begin{bmatrix} T_1 \\ \vdots \\ T_m \end{bmatrix} = \begin{bmatrix} g_1(O_1, O_2...O_7) \\ \vdots \\ g_m(O_1, O_2...O_7) \end{bmatrix}
\]

\[
\Delta \vec{T} = \vec{T} - \vec{T}_{baseline}
\]

\[
\vec{CD}_{DI} = \Delta \vec{T} S_{resist} + \vec{CD}_{baseline}
\]

• Seen as a constrained quadratic programming problem

Minimize

\[
\left( \vec{CD}_{DI} - \vec{CD}_{target} \right)^T \left( \vec{CD}_{DI} - \vec{CD}_{target} \right)
\]

Subject to:

\[
O_{Low} \leq O_i \leq O_{Up} \quad i = 1,2...7
\]
Final Inspection (FI) CDU Control Methodology

\[
\vec{CD}_{DI} = \Delta \vec{T} \; S_{\text{resist}} + \vec{CD}_{\text{baseline}}
\]

- Plasma etching induced AW CD bias (signature)

\[
\Delta \vec{CD}_{ps} = \vec{CD}_{FI} - \vec{CD}_{DI}
\]

- Across-wafer FI CD is function of zone offsets

\[
\vec{CD}_{FI} = \vec{CD}_{DI} + \Delta \vec{CD}_{ps} = \begin{bmatrix} g_1(O_1, O_2...O_7) \\ \vdots \\ g_n(O_1, O_2...O_7) \end{bmatrix}
\]

- Minimize:

\[
\left( \vec{CD}_{FI} - \vec{CD}_{target} \right)^T \left( \vec{CD}_{FI} - \vec{CD}_{target} \right)
\]

- Subject to:

\[
O^{Low} \leq O_i \leq O^{Up} \quad i = 1,2...7
\]
FI CDU Control Verification Experiment Setup

- Focus on Pitch 250 L/S 1:1, plate B
- Use two-week-average FICD and bias signatures to generate offsets
- Verification experiment is done sequentially
- PEB adjustment is checked first to ensure it is close to the model-predicted one
- DICD is then checked to ensure its correct adjustment
- FICD is finally checked
Long Term Overall Improvement ~35% in recently completed experiment at AMD/SDC across-wafer sigma of 250 1:1 lines, using CDSEM

Confirmation Wafers (done six months after calibration)

Before

After

\[ \sigma = 1.36\text{nm} \quad m = 141.9\text{nm} \]

\[ \sigma = 1.21\text{nm} \quad m = 142.1\text{nm} \]

\[ \sigma = 1.26\text{nm} \quad m = 141.7\text{nm} \]

\[ \sigma = 1.14\text{nm} \quad m = 141.5\text{nm} \]

\[ \sigma = 1.41\text{nm} \quad m = 141.4\text{nm} \]

\[ \sigma = 1.39\text{nm} \quad m = 142.4\text{nm} \]
Verification experiment results
(before control vs. after control)

DICD uniformity is sacrificed in order to optimize FICD uniformity

Qiaolin (Charlie) Zhang, on internship at AMD/ Spansion 2005-06
**Data Mining for Yield Ramping (APC)**

- **What is it:** Exploit existing tool/wafer data for control optimization

- **Basic Idea:**
  - Wafer Metrology alone has limited precision – enhance it by combining tool/process/wafer data using multivariate techniques
  - Identify basic operating fingerprints, and distinguish from fingerprints in “rogue” situations
  - Combine basic operating fingerprints to predictive models suitable for APC

- **Potential Payoff:**
  - Faster, more disciplined yield ramp
  - Rational deployment of metrology and control resources
  - Leapfrog present metrology precision/accuracy limitations
Example of Proposed Control Deployment

- **Incoming Wafer**
  - Physical Wafer Measurements
  - Process A Model
  - Model-based Controller
  - SPC & recipe Filter
  - Process A
  - Model Prediction of Physical and Electrical Wafer parameters

- **Process A**
  - Model-based Controller
  - SPC & recipe Filter

- **Process B**
  - Model-based Controller
  - SPC & recipe Filter

- **Production Metrology**
  - Model Maintenance
  - Control Decisions (supervisor decides on feedback/feed-forward)
  - Recipe Model Maintenance

- **Outgoing Wafer**
  - Control Limits driving control alarms
  - Process Specifications
  - Generate Corrections

- **Process A Model**
  - Process B Model

- **Model Prediction of Physical and Electrical Wafer parameters**
Virtual Metrology Preview

**Summary of Fit**

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<td>Observations (or Sum Wgts)</td>
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Outline

- CD Control
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- IC Performance Impact
- New Directions
Motivation

- Monte Carlo simulation:

  Canonical circuit

  \[ \mu_{sys}(x,y), \sigma_{rand}^2, (\rho_{\mu m}(\Delta x, \Delta y)) \]

  

  delay  

  power
Decomposition of Spatial CD Variation

Average Wafer + Scaled Mask Errors + Across-Field Variation

= Across-Wafer Variation + Die-to-Die Variation + “Random” Variation

Spatial Correlation & Process Control

- Calculation of spatial correlation, before and following decomposition of variance:

\[ z_i = \frac{(x_i - \bar{x})}{\sigma} \]

\[ \rho_{jk} = \frac{\sum z_j z_k}{n} \]

- Large (mm)-scale spatial correlation is largely accounted for by systematic variation; smaller, (\(\mu\)m)-scale correlation may still have structure, focus of current work.
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Digital Circuit Design and Sizing

• Digital Circuit Sizing Optimization Problem
  – Goal: size the gates in a combinational logic circuit
  – Minimize the effects of individual gate delay variations and spatial correlations on the overall circuit delay

• Previous Work: Geometric Programming approach†
  – Objective: \( \min \{ \max_{p \in \text{all circuit paths}} \sum_{i \in p} [\bar{D}_i + k \sigma_i(D)] \} \)
    where: \( D_i = \) nominal delay for gate \( i \)
    \( k = \) a constant \( \sim 2 \)
    \( \sigma_i(D) = \gamma (x_i^{-1/2}) \bar{D}_i \) derived from Pelgrom’s Model ††
    with \( \gamma \) model parameter
  – Constraints: Fixed maximum total circuit area


Performance Analysis

• 32-bit Ladner-Fisher adder circuit is sized and analyzed
  – 459 gates, 3214 paths from input to output gates

• Monte Carlo analysis with 5000 samples
  – RC model for nominal delay and a delay variation only due to $v_{th}$
  – Overall circuit delay statistics are compared under two designs:
    • Nominal Design, $\sigma = 0.88$
    • Statistical Design, $\sigma = 0.47$

• Limitations
  – gate delay variation depends only on $v_{th}$
  – Ignored spatial correlations between the gates

More Comprehensive Designs

• Adding delay variation dependence on $L_{\text{eff}}$ in the objective function:

$$\min\{\max_{p \in \{\text{all circuit paths}\}} \sum_{i \in p} [\bar{D}_i + k\sigma_i(D)]\}$$

where: $\sigma_i(D) = \gamma_{\text{th}}(x_i^{-1/2})\bar{D}_i + \gamma_{L_{\text{eff}}}(x_i^{-1/2})\bar{D}_i$

• Adding variation dependence on $L_{\text{eff}}$ and Spatial Correlation

$$\min\{\max_{p \in \{\text{all circuit paths}\}} \sum_{i \in p} [\bar{D}_i + k\sigma_i(D)] + k \sum_{i,j \in p, i \neq j} \rho_{ij}\sigma_i^2\sigma_j^2\}$$

where: $\sigma_i(D) = \gamma_{\text{th}}(x_i^{-1/2})\bar{D}_i + \gamma_{L_{\text{eff}}}(x_i^{-1/2})\bar{D}_i$

\[\rho_{ij} \equiv \text{spatial correlation between gate } i \text{ and } j \text{ with separation } d_{ij}\]

Large scale model

\[
\rho_{ij} = \begin{cases} 
1 - d_{ij} / X_L (1 - \rho_B) & d_{ij} \leq X_L \\
\rho_B & d_{ij} \geq X_L 
\end{cases}
\]

$X_L$ characteristic correlation length
$\rho_B$ characteristic correlation baseline
Monte Carlo Analysis on Circuit Delay

• 32-bit Ladner-Fisher adder circuit is analyzed
• Four types of Monte Carlo analysis are performed for each design

1. $\sigma(D) \sim \sigma(V_{th})$: gate delay variation results from $\sigma(V_{th})$

2. $\sigma(D) \sim \sigma(V_{th}) + sp.\ corr$: gate delay variation results from $\sigma(V_{th})$ and spatial correlations exist between the gates

3. $\sigma(D) \sim \sigma(V_{th}) + \sigma(L_{eff})$: gate delay variation results from both $\sigma(V_{th})$ and $\sigma(L_{eff})$

4. $\sigma(D) \sim \sigma(V_{th}) + \sigma(L_{eff}) + sp.\ corr$: gate delay variation results from $\sigma(V_{th})$, $\sigma(L_{eff})$ and spatial correlations exits between the gates
Simulation Results (5000 Monte Carlo Samples)

a) Deterministic design objective

b) Minimize delay variations due to $V_{th}$

c) Min. delay var. due to $V_{th}$ and $L_{eff}$

d) Min. delay var. due to $V_{th}$, $L_{eff}$ and Spa. Corr.
Simulation Results

• Focus on the last analysis which considers both delay variations due to $V_{th}$ and $L_{eff}$, and spatial correlations

a) Deterministic design
$\sigma(D) = 3.02$, yield = 63.42%

b) Minimize delay variations due to $V_{th}$
$\sigma(D) = 1.96$, yield = 92.06%

c) Min. delay var. due to $V_{th}$ and $L_{eff}$
$\sigma(D) = 1.52$, yield = 96.62%

d) Min. delay var. due to $V_{th}$, $L_{eff}$ and spatial correlation
$\sigma(D) = 1.36$, yield = 98.22%
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Matching Properties of MOSFETs

- Average value of the parameter over any area is given by the integral of \( P(x,y) \) over this area.
- Actual mismatch is given by the difference of two integrals

\[
\Delta P(x_{12}, y_{12}) = \frac{1}{\text{area}} \left\{ \int \int_{\text{area}(x_1, y_1)} P(x', y') \, dx' \, dy' - \int \int_{\text{area}(x_2, y_2)} P(x', y') \, dx' \, dy' \right\}
\]

- This integral can be interpreted as the convolution of a geometry function with the "mismatch source" function \( P(x,y) \)

\[
x_{12} = \frac{x_1 + x_2}{2}, \quad y_{12} = \frac{y_1 + y_2}{2}
\]

\[
\Delta P(x_{12}, y_{12}) = \frac{1}{\text{area}} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} P(x', y') G(x' - x_{12}, y' - y_{12}) \, dx' \, dy',
\]

\[
G(x', y') = \text{BOX} \left( x' - \frac{D}{2}, y' \right) - \text{BOX} \left( x' + \frac{D}{2}, y' \right)
\]

\[
\Delta P(\omega_x, \omega_y) = G(\omega_x, \omega_y) \cdot P(\omega_x, \omega_y)
\]

\[\text{BOX} (x, y) = \begin{cases} 1 & \text{for } x \in \left( -\frac{L}{2}, \frac{L}{2} \right), y \in \left( -\frac{W}{2}, \frac{W}{2} \right) \\ 0 & \text{else} \end{cases}\]

First Source of Variation – White Noise

- The events have a correlation distance much smaller than the transistor dimensions.
- In Fourier domain it is a constant value for all spatial frequencies

\[ \sigma^2(\Delta P) = \frac{1}{4\pi^2} \int_{\omega_y=-\infty}^{\omega_y=\infty} \int_{\omega_x=-\infty}^{\omega_x=\infty} \left| G(\omega_x, \omega_y) \right|^2 \cdot \left| P(\omega_x, \omega_y) \right|^2 \, d\omega_x \, d\omega_y \]

- The assumption of short correlation distance implies that no relation exists between matching and the spacing D between two transistors.

\[ \sigma^2(\Delta P) = \frac{A_p^2}{WL} \]

But what if W and L are also variable?
Additional Sources of Variation are Deterministic

- Systematic error from across wafer variations
- Systematic error from within field variations
  - Scanner optics / mechanics
  - Mask errors
  - Pattern densities (in Litho, Etch, CMP, Anneal, etc.)
  - And, of course, LER…

\[ \sigma^2 (\Delta P) = S_P^2 D_x^2 + ? \]

How do we deal with the complexity of the deterministic functions?
Device Model and Yield under LER

\[ P(L) = \frac{1}{\sigma_{LWR} \sqrt{2\pi}} e^{-\frac{(L-\langle L \rangle)^2}{2\sigma_{LWR}^2}} \]

\[ p_{x,s} = \int_{-\infty}^{l_{crit}} P(x') dx' = \frac{1}{2} \left[ 1 + \text{Erf} \left( \frac{L_{crit} - \langle L \rangle}{\sqrt{2\sigma_{LWR}^2}} \right) \right] \]

\[ P_{dev} = 1 - (1 - P_{seg})^{N_{dev}} \min[1, W / \xi] \]

\[ \text{yield} = (1 - P_{seg})^{N_{dev}} \]
FinFET LER

Body

Gate

\[ h \]

\[ t \]

\[ L \]
FinFET LER
FinFET LER Issues

- Hot carrier reliability
- Mobility degradation due to surface scattering
  - Si FinFET vs. TFT
- $I_{off}$ and $I_{on}$ variations due to LER
- Orientation effects
- Poly-Si vs. sc-Si
  - TFT vs. bulk
Transfer of LER

- Transfer of LER from resist film onto underlying film is a multi-step process
- Furthermore, the junction edges of tip and halo implants is redefine the LER underneath the etched gate stack

Schematic of a typical gate stack
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In Summary

• CD (and many other, equally critical elements) vary in a complex manner
• We are observability- and controllability-limited
• Major efforts are under way to
  – Enhance the metrology capability
  – Reform and expand the models of variability
  – Incorporate variability modeling into DFM tool

• We are bringing in enhanced CD metrology capability by the donation of the Timbre/TEL ODP tool