Current Milestones

• **Develop physical parameter isolating Process-EDA test structures (M17)**
  – Use physical models to design and measure test structures that identify and quantify key parameters in mask making, lithography (ASML-DUV), etching (Centura) and CMP (Berkeley Apparatus).

• **Benchmark PSM-PI against other methods on industrial tools (M18)**
  – Compare interferometric probe monitors for aberrations and illumination mapping with existing alternative technologies on industrial tools.

• **Evaluate and validate the DFM-LPD* software test-bed (M19 Rev)**
  – Design short-loop device test patterns, photomask tapeout, collaboration with Cypress on fabrication, SEM and electrical characterization and compare with predictions of the DFM-LPD testbed being developed at Berkeley on SRC/DARPA support.

• **Electrical Versions of Test Patterns (Added - Supplement)**
  – Create, design layout, process and perform initial electrical probing of promising electrical versions of test patterns for monitoring lateral influences of processes.

* DFM-LPD = Design For Manufacturing – Layout-Process-Device
Now called Quantitative Yield Simulator supported by SRC/DARPA
Pattern-And-Probe Characterization Technology

Garth Robins
PhD May 2005
Optics at Lockheed

Developed pattern-and-probe aberration monitors including target operation and relationship of sensitivity, cross-talk, to proximity, EM, mask making, ....

Experimentally demonstrated and developed the quantitative usefulness of targets in industrial practice and science in collaboration with industry and colleagues.
High-NA and Polarization Monitors

Greg McIntyre

- Polarization aberrations: compared various representations and proposed a common ‘language’ to describe them
- Polarization monitoring: gained experimental verification of monitoring polarization with phase shift masks
- Pattern matching: developed technique to screen IC layouts for areas most vulnerable to polarization and high-NA effects using pattern matching
Polarization Aberrations: Physical Mechanisms

Diattenuation: attenuates eigenpolarizations differently (partial polarizer)

Retardance: shifts the phase of eigenpolarizations differently (wave plate)

Total representation of pupil has 8 degrees of freedom

- Apodization
  - Magnitude
  - Eigenpolarization orientation
  - Ellipticity of eigenpolarization
- Scalar aberration
  - Magnitude
  - Eigenpolarization orientation
  - Ellipticity of eigenpolarization
- Diattenuation
- Retardance

However, this format is
- inconvenient for understanding impact on imaging
- inconvenient as an input format for simulation
The advantage of the Pauli-Pupil Jones

- 8 coupled pupil functions
  (easy to create unrealizable pupil)
- 128 Zernike coefficients
- not very intuitive
- fits imaging equations

Pauli

- 4 independent pupil functions
  (scalar effects considered separately)
- 64 Zernike coefficients
- physically intuitive
- easily converted to Jones for imaging equations

Proposed simulation flow

Input: \( a_1, a_2, \) scalar aberration

\[
\begin{align*}
\sigma_1 & = \sigma_2 = \sigma_3 = 0 \\
\theta & = \rho \\
\end{align*}
\]

Calculate \( a_0(\text{real}) \)

\[
J(H, \rho, \theta) = a_0\sigma_0 + a_1\sigma_1 + a_2\sigma_2 + a_3\sigma_3
\]

User can vary input parameters and not have to worry about creating an unreal pupil

09/15/2005

FLCC - Lithography
PSM Polarimetry: Monitoring polarization with phase shift masks

- Set of 6 phase shift monitors form a polarimeter
- Intensity in center of image is polarization dependent

\[ S_m = W^{-1}F \]

- Measured values
- Calibration matrix
- Measured Stokes vector

- Next test mask is being fabricated in collaboration with Benchmark Technologies and Dupont with an array of pinholes in the backside to ensure coherent illumination for all frequencies
PSM Polarimetry: Experimental results from Photronics 4-phase FLCC mask

Polarization sensitivity is observed in generation 1 patterns (radial phase grating, exposed on Nikon development tool)

<table>
<thead>
<tr>
<th>Incident Light</th>
<th>Clearing dose</th>
<th>%CF</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>1.88</td>
<td>0.52</td>
</tr>
<tr>
<td>Un</td>
<td>2.76</td>
<td>0.36</td>
</tr>
<tr>
<td>Y</td>
<td>4.75</td>
<td>0.23</td>
</tr>
</tbody>
</table>

Fraction of clear field

- X pattern: Clearing dose 1.88, %CF 0.52
- Un: Clearing dose 2.76, %CF 0.36
- Y: Clearing dose 4.75, %CF 0.23

Flux measurement vs. incident light

3 periods, NA<sub>des</sub> = 0.56, applied bias 40nm

09/15/2005 FLCC - Lithography
Screening Layouts for Vulnerabilities to Polarization and High-NA: Concept

Tool Conditions ($\lambda$, NA, $\sigma$, $E_{ox}$:$E_{oy}$, aberrations, …)

Lithographer

Pattern Generator

Patterns ($P_x$, $P_y$, $P_u$)

Theory

Match Location(s) & Match Factor(s)

Pattern Matcher

Vulnerability Scores ($V_{Pol}$, $V_{NA}$, $V_{defocus}$, $V_{z5}$, …)

Modify Layout or further investigation

Mask Layout

Designer

09/15/2005

FLCC - Lithography
Fast-CAD and Novel Targets

Student-Test Mask Coordinator
Pattern Matching Extensions
• High-NA
• Polarization
• Strong Off-Axis
• Double Exposure
• Device Variability

Novel Targets
• Electrical Probing
• Electronic detection

Juliet Holwill
CAD Student
Modifications to Pattern Matcher for High-NA and Polarization

- Multiple match factors were required to calculate the vulnerability scores. This was calculated as a post-processing step.
- The output was converted to a dscript format to be input to the Panoramic simulator.
- The performance depends on the number of match factors required and how many matches are found.

Match Location and snippet in SPLAT format

- Convert to dscript format
- Output Match Factor
- More match factors?
  - yes
  - no → Done

09/15/2005 FLCC - Lithography
Vulnerability to Perturbations of Illumination Polarization State
(Coherent Illumination, Alternating PSM, fabricated examples)

Vulnerability score ($V_{\text{pol}}$) is a good predictor of how susceptible the layout is to variations in polarization ($V_{\text{pol}} \propto I_X - I_Y$) relationship.

\[
V_{\text{Pol}} = \frac{\partial I_{\text{p}}}{\partial E_{\text{ox}}}
\]

### Intensity vs. Vpol Score (for each polarization state)

- **Intensity at Point**
  - X pol
  - Y pol
  - X-Y

### Vulnerability score (Vpol) vs change in intensity for 10% polarization variation
Electrical Testing for Aberration Monitoring

The interferometric pattern and probe targets produce varying intensities, depending on aberration magnitude.

These variations can be used to create an open circuit when a lens aberration is above a certain threshold.

**Step 1:** Silicon wafer is oxidized to form a thin pad oxide layer of SiO$_2$.

**Step 2:** Deposit thin film of metal (Al or Ti)

**Step 3:** Expose all areas but dogbone with positive photoresist

**Step 4:** Second double exposure with test pattern

**Step 5:** Develop resist and etch metal
Abacus Layout
Greg McIntyre, Polarization
Jing Xue
Juliet Holwill, Electric Test
Willy Cheung, Linewidth Metrology
Garth Robins, Aberration Monitors
Wojtek Poppe, Grid Size Investigation

New Design
Alignment Tolerance
100 um

Juliet Holwill, Electric Test
09/15/2005
Results and Current Activities Year 2

- **Develop physical parameter isolating Process-EDA test structures**
  - Juliet Holwill: Integrated Multi-Student Test Mask (Aug 05 Tape Out)
  - Greg McIntyre: Designed new back-side pin-hole mask with Benchmark/DuPont

- **Benchmark PSM-PI against other methods on industrial tools**
  - Garth Robins: Completed PhD; 193 nm measurements and critical assessment
  - Greg McIntyre
    - Finished 2nd round of experiments on high-NA polarization as intern at AMD and in collaboration with NIKON.
    - Tutorial paper on representations of polarization and choice for CAD

- **Evaluate and validate the DFM-LPD software test-bed**
  - Juliet Holwill: Extended Pattern Matcher code to high-NA and polarization
  - Juliet Holwill and Greg McIntyre simulation validation (high-NA, Pol)
  - Wojtek Poppe (SR/DARPA): ATT-PSM shuttle mask being processed in Short Loop NMOS run at Cypress

- **Electrical Versions of Test Patterns**
  - Juliet Holwill created new designs and layouts that suppress ring sidelobes and this enable automatic electrical probing of opens and shorts for wafer mapping.
Design-Rule Qualifiable Test-Structures for Nominal Process Parameters

Challenge:
- OPC/PPC parameters must be tuned to the Fab. often even without knowledge of the NA, illumination, etc. (Just Design Rules)

Hypothesis:
- Versions of 2D Test Patterns could be implemented that pass DRC and are significantly (3X) superior to device features in isolating and quantifying OPC/PPC parameters.

Research Strategy:
- Implement Patterns similar to FLCC Test Patterns with feature sizes ~ 0.5 λ/NA.
- Use simulation to optimize promising layouts
- Validate in collaboration with industry
Fast-CAD Pattern Matching Extensions
New Tools to find and quantify
Worst Case Locations Fast

Juliet Holwill
Eric Chin

• Local Effects (Poly)
  – Local Layout
  – Gate Vt and Leakage
  – Advanced Lithography (Pol., high off-axis, double exposure)
  – Residual LWV propensity

• Global Effects (Metal)
  – Net List and Chip Location
  – Lens slit position variation
  – CMP dishing variation

Maximal Lateral Impact Function

Convert to dscript format

Output Match Factor

More match factors?

yes
no

Done
DuPont Mask

Cypress Poly Block

Metal Active Center Poly Contact Quasar OPC Poly Corner Poly

Cypress DDLI Block

Platform for Collaborative DFM
Modeling SRC/DARPA and experiment FLCC

10 pad cells:
3 line array
SRAM
Inverter
NAND
Adder Misalignment

Cypress Semiconductor chip will help identify sources of variation in transistor leakage across die, field, wafer and lot as well as validate Quantitative Yield Simulator (QYS).

Full adder:
10 pads
6 gates
16 transistors

Testing leakage of only one gate at a time

Source 1 Source 2 Drain 1 Drain 2
Shot Noise: Now DARPA 13 mo

Acid Generation

Acid Diffusion/Reaction

Marshall Miller

Statistical Modeling

Combined = \frac{\sqrt{VAR}}{AVE} = \sqrt{\frac{1}{N_1} + \frac{1}{N_2} + \frac{1}{N_3}}

Linewidth Variation

Electronic Mechanical View

Statistical Analysis

Dissolution Modeling

Quencher Combination

Contactor Arrays

Acid Strength

150nm

As-split surface
Future Milestones

• Establish industry acceptable Process-EDA test structures (LITH Y3.1)
  Refine test-patterns designs to measure key model parameters while mitigating chip test area, minimize mask-writing time, and maximize simplicity in quantitative interpretation.

• Create design-rule qualifiable test structures for PPC calibration (LITH Y3.2)
  Create 2-D test patterns that are compatible with design rules and superior to device features in identifying and quantifying process parameters for pre-compensation treatments.

• Test electrical PSM-PI and explore zero-foot-print electronic versions (LITH Y3.3)
  Evaluate wafer performance of electrical probe PSM-PI for focus mapping. Combine parameter specific interferometric-probe targets with electronic detection and RF communication for in situ stepper measurements.

• Evaluate Pattern-Matching for predicting device variation hot-spots (LITH Y3.4)
  Develop maximum lateral impact functions for locating gates with high levels of device variation and correlate results with wafer experiments and the Quantitative Yield Simulator being developed on SRC/DARPA support.

• Prototype Pattern-Matching for predicting interconnect delay variation (LITH Y3.5)
  Develop maximum lateral impact functions and net-list tracking software for locating, quantifying and summing variations in interconnect delay due to residual process non-idealities.