Feature-level Compensation & Control

Workshop
September 13, 2006

A UC Discovery Project
Current Milestones

- **Establish industry acceptable Process-EDA test structures (LITH Y3.1)**
  Refine test-patterns designs to measure key model parameters while mitigating chip test area, minimize mask-writing time, and maximize simplicity in quantitative interpretation.

- **Create design-rule qualifiable test structures for PPC calibration (LITH Y3.2)**
  Create 2-D test patterns that are compatible with design rules and superior to device features in identifying and quantifying process parameters for pre-compensation treatments.

- **Test electrical PSM-PI and explore zero-foot-print electronic versions (LITH Y3.3)**
  Evaluate wafer performance of electrical probe PSM-PI for focus mapping. Combine parameter specific interferometric-probe targets with electronic detection and RF communication for in situ stepper measurements.

- **Evaluate Pattern-Matching for predicting device variation hot-spots (LITH Y3.4)**
  Develop maximum lateral impact functions for locating gates with high levels of device variation and correlate results with wafer experiments and the Quantitative Yield Simulator being developed on SRC/DARPA support.

- **Prototype Pattern-Matching for predicting interconnect delay variation (LITH Y3.5)**
  Develop maximum lateral impact functions and net-list tracking software for locating, quantifying and summing variations in interconnect delay due to residual process non-idealities.
PSM Polarimetry: Monitoring polarization at 193nm high-NA with phase shift masks

Greg McIntyre
PhD May 06

- Multi-phase mask patterns derived from high numerical aperture theory to sample illumination polarization states. Used to assess layout sensitivity.
- Multiple patterns work together to characterize polarization

- Backside pinhole enables frequency selection and full pupil-fill measurement
Full pupil-fill polarization characterization

Collaboration with Benchmark Technologies, Toppan, AMD and Nikon

Angle selection with pinhole array on backside of reticle

513 pinhole / cluster combinations
- 3 types of ‘OPC’
- 2 pinhole sizes
- 9 programmed pinhole misalignment
- 9 programmed process misalignment
- 5 calibration & 4 test exposed polarization states

Collaboration with Benchmark Technologies, Toppan, AMD and Nikon
Phase Shift Mask Interferometric Birefringence Monitor

Greg McIntyre

Does industry need electrical versions of polarization monitors?
EM effects in masks, inspection and novel monitors

- Characterize PSM mask opening cross talk
- Develop analysis methodologies for surface roughness generated noise in inspection
- Explore novel guided-wave and plasmon CD and LER monitors.

DARPA Shot Noise => FLC

Marshal Miller
EM Simulation

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FLCC - Lithography
EM Topography Effects

- ATT-PSM and CPL Mask Opening Cross-Talk
  - Use TEMPEST time-evolution to visualize cross-talk as it occurs among masks openings
  - Introduced reduced parameter edge and line source models

- Noise in Inspection
  - Utilize fields in smooth structures to estimate noise sources
  - Utilize partial coherence to reduce summation effort

Build on Kostas Adam’s work
EM Topography Effects (Cont.)

High Q guided wave resonator structure

Changes in duty cycle affect coupling
Variations in CD affect Q
LER produces out of plane scatter

• Guided-wave Monitors for CD’s and LER
  – Identify high Q optical guiding structures as test vehicles
  – Evaluate sensitivity of angle and bandwidth (Q) of optical coupling into guides to duty cycle, duty cycle spread, and LER
Fast-CAD and Novel Targets

Pattern Matching Extensions
- High-NA
- Polarization
- Attenuated-PSM
- Strong Off-Axis
- Double Dipole Exposure

Novel Targets
- Electrical Probing
- Electronic detection

Student-Test Mask Coordinator

Juliet Holwill
CAD Student

50/50 FLCC/SRC
Aberration Monitoring with Electrical Testing

Contact Pad + Thin line of conductive material = Open circuit created when aberration present

Defocus = 0.0  Defocus = 0.02  Defocus = 0.2
Single Exposure Results: Focus Exposure Matrix

- Focus Steps: 0.04um +

Process Conditions:

NA = 0.85
λ = 193nm

Double exposure results soon to come!
Automatic Generation of Design Rule Compatible Monitors

- Automate the generation process
- Include input patterns for focus, illumination, high-NA, polarization
- Evaluate the change in sensitivity and selectivity vs. design rules
- Extend to evaluating and generating 2D targets suitable for OPC calibration

Focus examples
Design-Rule Qualifiable OPC Characterization Methodologies

- OPC calibration is a current challenge to the industry as with each process change the calibration must be done cost effectively and accurately to maintain a high degree of predictably in pattern compensation.
- Morph parameter specific theoretical test patterns into circuit-like patterns and characterize the retention of their sensitivity and selectivity to key exposure and resist parameters.
- Use Pattern Matching to derive from a layout a complete catalog of pattern primitives.
- Then use the test patterns and catalog of primitives to evaluate weakness in model based approaches and the completeness of patterns sets in empirical approaches to OPC calibration.
  - Make systematic studies of the weakness in physical modeling approaches based on our resist modeling experience with STORM and Prolith.
Extension of Fast-CAD Pattern Matching for Assessing Across Chip Interconnect Variation

New Chip Level Tools to Find and Quantify Location Dependent Variations of R and C

Eric Chin

50/50 FLCC/SRC

- Quantify and Paraeto Physical Causes
  - Alignment, Plasma Etch, slit position, CMP dishing variation
- Assess feasibility of software functions
  - Net List, Chip Location
- Define Architecture

 Capacitance Variation Function

Multiple Mask Level Operator

Follow Wiring and Location

More Wiring to Follow?

yes

no

Done

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Modification of Extracted Parasitics

Pattern Match

Calculate Edge Movements

Determine $\Delta R, \Delta C$

Modify Extracted Values

Match Factor [-1,1]

Original

New

```
*JNET CLKGigoEn 1.10227e-16
*IP (CLKGigoEn 0 0.0 9814500 5400)
C1 CLKGigoEn:ck_en 0 1.0278e-16
R1 CLKGigoEn:ck_en CLKGigoEn 5.2149e-12
```

```
*JNET CLKGigoEn 1.10227e-16
*IP (CLKGigoEn 0 0.0 9814500 5400)
C1 CLKGigoEn:ck_en 0 1.09293e-16
R1 CLKGigoEn:ck_en CLKGigoEn 3.91214e-12
```
Design Flow

- Process Technology: ST Micro CMOS090
- Collaboration with the Berkeley YODA Group

FAIL, Respin Design

Parasitic Extraction

Pattern Matcher

Delay Prediction

Timing Analysis

PASS, Proceed to Next Step
Fast-CAD Modeling of Additional Processing Effects

Collaboration: Jihong Choi CMP modeling and Eric Chin Lithography and DFM

- CMP Dishing and Erosion
  - Density Dependent Thickness Variation

\[
\frac{dz}{dt} = \frac{K}{\rho(x,y)} = - k_p P v
\]

- Misalignment
  - Capacitance Variation

\[
C_{WIRE} = C_{PP} + C_{FRINGE} \approx \frac{w \varepsilon_{di}}{t_{di}} + \frac{2\pi \varepsilon_{di}}{\log(t_{di}/H)}
\]
Manufacturing Effects on Standard Design Styles

• Assist in electrical testing of Cypress wafers (FLCC)
• Use Pattern Matching to identify severity of cell to cell interactions in Standard Cells (FLCC)
• Prototype novel process aware EDA tools that do not burden the designer (SRC)

Lynn Wang
CAD Student

50/50 FLCC/SRC
Research Plan

• Automate an assessment process that determines the severity of OPC effects between circuit elements in a library (FLCC).

• Assess the speed and accuracy of the Pattern Matching approach for this purpose (FLCC).

• Prototype EDA tools for visualizing and fixing vulnerable spots (SRC).

Patterns of tri-foil and coma matched on 0° and 180° FPGA layout.
Visualizing Statistics of Many Cases

**SPLAT delta E vs. Match Factor**
- Interaction level characterization
- Interaction distance characterization
- Lithography strategy characterization (i.e. top hat, annular, quadrupole, soft dipole, etc.)
- Validation with SPLAT by examining the correlation between image change and match factors

**Interaction Level Characterization**

Mock Data Only
Questions to be Addressed

- Do the match factors of spillovers exhibit significant change due to the presence of adjacent standard cell blocks?
- How do the magnitudes of the spillovers change by varying the distances of standard cell blocks?
- Can we extract guidance from good/bad cells and good/bad neighbors to minimize these spillovers regardless of adjacent cells?
Experiments on Sources of Variation

Wojtek Poppe
SRC/DARPA

2005 and 2006 Test Mask Designs
Enhanced NMOS at Cypress
Measure Vt and Leakage at UCB

Vary: Focus; Dose; Illumination; OPC

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FLCC - Lithography
Cypress/DuPont Experiments

Device

Finding correlation between gates

Characterizing your process

Process

Circuits built to measure circuit variations

Using device design to measure CD variation

Super low power design

Finding correlation between gates

Random and regular

RANDOM

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FLCC - Lithography
Enhanced Transistor CD Metrology

A 7X increase in slope after a 10X increase in implant dose

<table>
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<tr>
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<th>Gate CD</th>
<th>Gate Oxide Thickness</th>
<th>Channel Doping</th>
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<tbody>
<tr>
<td>Ioff sensitivity enhancement</td>
<td>2500%</td>
<td>750%</td>
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Build table from measured data

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<thead>
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<th>dose (mJ/cm²)</th>
<th>CD (nm)</th>
<th>Ioff (A)</th>
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</table>

FLCC - Lithography

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Over 10,000 Individually Probable Transistors and Test Structures

Liang Teck’s Structures

Defocus Target

Pass Transistor Logic

Non-rectangular gate

Corner rounding

Good and bad ILS

FLCC - Lithography

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Streamlined Multi-Designer Chip Creation Flow

178 30-pad cells

Ready for many more contributors on next chip
The SRC Process Aware EDA Tool Kit Team and Rectangle Pushing Strategies

Wojtek Poppe  Lynn Wang  Eric Chin  Juliet Holwill  Jae-Seok Yang

Robustness  Interconnect  Lateral Image  Interactions & Placement  Crosstalk

Metric  Delay  Interactions & Placement

- quantifying the circuit performance robustness of layout snippets with an indexing metric
- control of leakage through maximizing optical image quality of drivers/buffers,
- mitigating optical spillover effects and optimizing robustness metrics in placement,
- visualizing chip level effects on delay variation, and
- checking robustness closure through estimating variations in interconnect.
We want to make each step of the physical design flow process-aware.

We need to propose an efficient method of incorporating manufacturability and yield information in each of the cost estimation steps to allow optimization in the earlier part of the design flow.

We propose to implement a method for estimating cost to guide the flow by using pattern matching techniques.

We eliminate the need for post-layout corrections.
Future Milestones

- **Build a web-based, interactive platform for collaborative analysis of variation.** *(LITH Y4.1)*

Assemble current in-depth understanding, catalog SEM and electrical measurements versus wafer position, and facilitate on-line statistical queries of simulation and experimental data to promote collaborative prediction and analysis of sources of nonuniformity in Semiconductor Manufacturing.

- **Make electrical measurements and perform statistical analysis of wafer data.** *(LITH 4.2)*

Make electrical and SEM measurements of fabricated leakage test circuit patterns from Cypress and correlate mean and variance with layout and programmed treatments and simulation predictions.

- **EM effects in masks, inspection and novel monitors.** *(LITH 4.3)*

Characterize PSM mask opening cross talk, develop analysis methodologies for surface roughness generated noise in inspection, and explore novel guided-wave and plasmon CD and LER monitors.
Future Milestones (Cont.)

• **Evaluate design-rule qualifiable OPC characterization methodologies (LITH 4.4)**
  Morph parameter specific theoretical test patterns into circuit-like patterns and characterize the retention of their sensitivity and selectivity to key exposure and resist parameters. Use Pattern Matching to derive from a layout a complete catalog of pattern primitives. Then use the test patterns and catalog of primitives to evaluate weakness in model based approaches and the completeness of patterns sets in empirical approaches to OPC calibration.

• **Demonstrate accuracy and speed of Pattern-Matching for hot-spots (LITH Y4.5)**
  Compare estimates of linewidth shape and device leakage from Pattern Matching with full lithography simulation and the Quantitative Yield Simulator being developed on SRC/DARPA support for both custom and standard design styles.

• **Demonstrate accuracy and speed of Pattern-Matching for predicting interconnect delay variation (LITH Y4.6)**
  Compare Pattern Matching estimates of interconnect delay variation including full chip CMP modeling with brute force modeling.