Feature-level Compensation & Control

FLCC

Workshop
September 13, 2006

A UC Discovery Project
Current Milestones (Year III, 1/27/06 to 1/26/07)

• Complete experimental study for CD non-uniformity reducing across the litho-etch sequence (SENS Y3.2)
  – Experimentally verify DI & FI CDU improvement using model based optimal control of PEB with various CD objective functions.

• Using Spatial CD Correlation in IC Design (SENS Y3.3)
  – Develop test structures and measurement plans for extracting spatial correlation characteristics.

• Aerial Image Metrology (SENS Y3.4)
  – Complete the micro-assembly of the commercial CCD with the Si carrier wafer. Integrate the aperture mask and the CCD arrays.

• Modeling and demonstration of metrology wafer for detection and thin-film roughness monitoring.
  – Initiate prototyping of wireless data acquisition/transmission and evaluate performance with measurements made in experimental systems.
Zero-footprint Optical Metrology Wafer – Prototyping and Modeling

Students: Vorrada Loryuenyong and John Gerling

Faculty: Professor Nathan Cheung
Motivation

- Real-time monitoring in hostile processing environments such as in plasma, wet etching, and CMP
- End-point mapping
- Mechanism studies of wet and dry processes
- Self-contained metrology unit with power and wireless or wired I/O.
Wet Etching Experimental Setup

- GaN-based LED is used for real-time, reflection-based measurement
- The signals at the output must separate the signal of interest from the noise floor
- The etchant droplets were transparent and have negligible effects on the data signals
Cu Etching vs. Window Alignment

**Experimental Condition:** Sputtering deposition, etching solution: Cyantek CR-7 (Perchoric based), nitride window thickness 649 ± 10nm + 500µm quartz slide, LED peak wavelength 463 ± 15nm, Cu thickness 60-70nm. $\theta_i =$ incident angle, $\theta_r =$ reflective angle.

- Window misalignment will reduce light intensity that would contribute to the optical signal
- Etching rate ~ 8-10 nm/s
Photoresist Wet-Etch

Experimental Conditions

- LED peak wavelength $463 \pm 15$ nm
- Substrate: Pyrex glass $520-540 \, \mu m$
- Spin-Coating: OCG OIR-897 and thick resist SPR220
- Etchants: OPD4262 developer and photoresist stripper PRS3000

* The optical images were taken with separated experiments without LED light.
** The data signals were normalized with the signals at $t = 120$ sec

- The optical signals can be used to detect the photoresist wet-etch process
- Pre-endpoint detection is difficult to be achieved due to non-dissolving photoresist in the etching solutions
High-Brightness (HB) LEDs

LEDs on Sapphire & Si

Advantages of HB LEDs
- Low power consumption
- High brightness
- Other feasible applications: photo-enhanced chemical etching

<table>
<thead>
<tr>
<th></th>
<th>LED on sapphire</th>
<th>LED on Si (lateral)</th>
<th>LED on Si (vertical)</th>
<th>HB LED</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V at 20mA</strong></td>
<td>4.2</td>
<td>4.0</td>
<td>3.8</td>
<td>2.7</td>
</tr>
<tr>
<td><strong>V at 100mA</strong></td>
<td>6.5</td>
<td>5.5</td>
<td>4.5</td>
<td>3.19</td>
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<tr>
<td>FWHM</td>
<td>30nm</td>
<td>34nm</td>
<td>34nm</td>
<td>20-40nm</td>
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LEDs on Cu*

*LEDs provided by SemiLEDs™
Summary

- Bottom reflection approach is advantageous than top reflection for etching environment.
- Simulation indicates roughness and lateral pattern monitoring are possible.
- Higher signal-to-noise ratio can be achieved with high-brightness LED

2006-2007 Main Objectives

- Increase signal level with high-brightness LED setup
- Prototyping the self-contained metrology unit with wireless I/O.
Milestones (SENS Y3.1)

- Modeling and demonstration of metrology wafer for detection and thin-film roughness monitoring.
- Initiate prototyping of wireless data acquisition/transmission and evaluate performance with measurements made in experimental systems.

Current Achievement

- Demonstrated a prototype wafer with $3 \times 3$ metrology cells.
- Investigated both metal and photoresist wet etching monitoring.
- Simulation indicates thin film roughness monitoring and lateral pattern monitoring are possible.

Updated Year 4 Milestones

- Simulation and experimental verification of lateral patterns detection (New Milestone)
- Demonstrate real-time monitoring of rapid wet etch processes (New Milestone)
Integrated Aerial Image Sensor (IAIS)

• Students: Jing Xue, Chaohao Wang, James Cheng

• Faculty: Costas J. Spanos
Integrated Aerial Image Sensor (IAIS) Concept

Dark contact mask forming a series of spatial frequency shifting apertures. On-wafer photo-detectors to detect the optical signal captured by the aperture mask.
IAIS Modeling

Aerial Image and Detector Image Reconstruction:

1. Discretize illumination source
2. Mask and projection optics simulation
3. Extract scattering orders at wafer plane
4. IAIS aperture mask simulation
5. Combine partial image to total detector image

Modeling Concept for Partially Coherent Imaging

Annular Illumination: s = 0.89/0.59, NA=0.85, BIM, CD = 65nm
Defocus Simulation:

Aerial Image 65nm L/S. Precision of determination of focus plane on the level of 10nm, with $I_{\text{dark}}=10\text{pA/cm}^2@25^\circ\text{C}$, $n_{\text{read}}=15$ electrons, QE = 0.5

* Noise magnified 200 times in the above plots
Modeling Transmission and Contrast

Light transmission of aperture mask is significantly higher in immersion compared to dry litho. Contrast has comparable values in dry and immersion settings.

(Immersion liquid is assumed to fill the trenches of the interference mask.)
Modeling Polarization Ratios

* Red curve: dry
* Blue curve: immersion.

Polarization ratio as a function of aperture mask material and geometry;
Aperture mask in Immersion system has much higher polarization ratio
Small chip is co-planar to the wafer carrier with the maximum height difference 1.17mm, and tilt angle 0.009°.
IAIS Aperture Mask Patterning

200nm aperture 100nm aperture

200nm and 100nm aperture mask pattern by e-beam lithography and plasma etch, designed for the 0.6mm aerial image testing system
IAIS Prototype

Circuit connection

Aperture mask pattern
2006 Main Objective

• Complete the micro-assembly of the commercial CCD with the Si carrier wafer. Integrate the aperture mask and the CCD arrays (year III milestone: 1,27,2006 – 1,27,2007)
  – On target
• Complete the liquid assembly and polymer assembly to integrate CCD chips to wafer carrier
  – Done
• Complete the aperture mask pattern on CCD chips by e-beam lithography for 193nm/248nm stepper
  – On target
• Complete the defocus analysis to predict the ability of IAIS calibration
  – Done
Aerial Image Sensor, Year IV

- Our work during year 3 proceeded in two parallel paths:
  - a) in continuing simulations (to refine the design and validate various masking approaches), and
  - b) in assembly, with the objective of having a working, wired prototype for i-line and 248nm operations.
- Next year we would like to bring this work to its conclusion by performing a series of experiments using our prototypes, with the objective of examining the efficacy of capturing mask and optical system issues.
  - These would include critical dimension control, focus/exposure control and basic system aberrations.
- Finally, at the conclusion of our studies about the various components of the system, we would like to undertake the “ideal” design, involving custom built detectors with the appropriate DUV sensitivity, that are using their own metal layer as the built-in interference mask.
  - This design will focus on a custom chip (or wafer) that would need only the supply of power in order to operate as a fully integrated, wireless aerial image detector suitable for the 42 to 20nm nodes.
  - It is unclear whether this particular design will actually be implemented during this fourth year, but a subsequent implementation project is possible.
CD Uniformity Control Across Litho-etch Sequence

Student: Qiaolin (Charlie) Zhang

Faculty: Kameshwar Poolla, Costas Spanos
2006 Main Objectives

✓ Complete preliminary experimental study for CD non-uniformity reducing across the litho-etch sequence (M27 YII.17)
  ✓ Assess predictive capability of mode, and build optimizing software to compute optimal changes in control parameters.
  ✓ Provide proof of concept test of CD non-uniformity.
  ✓ reduction scheme based on direct CD metrology.
Our Approach

• Compensate for systematic across-wafer CD variation sources across the litho-etch sequence using all available control authority:
  – Exposure step: die to die dose
  – PEB step: temperature of multi-zone bake plate
  – Etch: backside pressure of dual-zone He chuck
Develop Inspection (DI) CDU Control

• DI CD is a function of zone offsets

\[ \vec{T} = \begin{bmatrix} T_1 \\ \vdots \\ T_m \end{bmatrix} = \begin{bmatrix} g_1(O_1, O_2...O_7) \\ \vdots \\ g_m(O_1, O_2...O_7) \end{bmatrix} \]

\[ \Delta \vec{T} = \vec{T} - \vec{T}_{\text{baseline}} \]

\[ \vec{CD}_{DI} = \Delta \vec{T} S_{\text{resist}} + \vec{CD}_{\text{baseline}} \]

• Seen as a constrained nonlinear programming problem

• Minimize

• Subject to:

\[ \left( \vec{CD}_{DI} - \vec{CD}_{\text{target}} \right)^T \left( \vec{CD}_{DI} - \vec{CD}_{\text{target}} \right) \]

\[ O^{Low} \leq O_i \leq O^{Up} \quad i = 1, 2...7 \]
Final Inspection (FI) CDU Control

- Plasma etch signature:
  \[
  \Delta \vec{CD}_{p\_s} = \Delta \vec{CD}_{FI} - \vec{CD}_{DI}
  \]

- Across-wafer FI CD is function of zone offsets

\[
\vec{CD}_{FI} = \vec{CD}_{DI} + \Delta \vec{CD}_{p\_s} = \begin{bmatrix}
  g_1(O_1, O_2 \ldots O_7) \\
  \vdots \\
  g_n(O_1, O_2 \ldots O_7)
\end{bmatrix}
\]

- Minimize:

\[
\begin{pmatrix}
  \vec{CD}_{FI} - \vec{CD}_{target}
\end{pmatrix}^T
\begin{pmatrix}
  \vec{CD}_{FI} - \vec{CD}_{target}
\end{pmatrix}
\]

- Subject to:

\[
O^{Low} \leq O_i \leq O^{Up} \quad i = 1, 2 \ldots 7
\]
Verification experiment results
(before control vs. after control)

DICD uniformity is sacrificed in order to optimize FICD uniformity

Qiaolin (Charlie) Zhang, on internship at AMD/Spansion 2005-06

09/13/2006 FLCC - Sensors and Control
Spatial Modeling of Gate Length Variation

Students: Paul Friedberg, Qian Ying Tang, George Cheng

Faculty: Costas J. Spanos
Motivation

• Manufacturing-induced variation in device parameters leads to variability in circuit performance
• Two approaches to address this concern:
  – Tailor IC design to minimize sensitivity to parameter variation
  – Use process control to reduce manufacturing variation
• Investigate these approaches through Monte Carlo analysis of canonical circuits
• For accurate, useful predictions, Monte Carlo framework must model reality very well
  ➔ Specific focus of this work: detailed spatial variation of gate length
Spatial Correlation & Process Control

- Calculation of spatial correlation, before and following decomposition of variance:
  \[ z_i = \left( x_i - \bar{x} \right) / \sigma \]
  \[ \rho_{jk} = \frac{\sum z_j \cdot z_k}{n} \]

- Large (mm)-scale spatial correlation is largely accounted for by systematic variation; smaller, (\(\mu\)m)-scale correlation may still have structure, focus of current work
Digital Circuit Design and Sizing

• Digital Circuit Sizing Optimization Problem
  – Goal: size the gates in a combinational logic circuit
  – Minimize the effects of individual gate delay variations and spatial correlations on the overall circuit delay

• Previous Work: Geometric Programming approach†
  – Objective: \( \min \{ \max_{p \in \{ \text{all circuit paths} \}} \sum_{i \in p} [\overline{D}_i + k \sigma_i(D)] \} \)
    where: \( D_i = \) nominal delay for gate \( i \)
    \( k = \) a constant \( \sim 2 \)
    \( \sigma_i(D) = \gamma (x_i^{-1/2}) \overline{D}_i \) derived from Pelgrom’s Model†† with model parameter \( \gamma \)
  – Constraints: Fixed maximum total circuit area


More Comprehensive Designs

• Adding delay variation dependence on $L_{\text{eff}}$ in the objective function:

$$\min \left\{ \max_{p \in \{\text{all circuit paths}\}} \sum_{i \in p} [D_i + k \sigma_i(D)] \right\}$$

where: $\sigma_i(D) = \gamma_{th}(x_i^{-1/2})D_i + \gamma_{L_{\text{eff}}}(x_i^{-1/2})D_i$

• Adding variation dependence on $L_{\text{eff}}$ and Spatial Correlation

$$\min \left\{ \max_{p \in \{\text{all circuit paths}\}} \sum_{i \in p} [D_i + k \sigma_i(D)] + k \sum_{i,j \in p, i \neq j} [\rho_{ij} \sigma_i^2 \sigma_j^2] \right\}$$

where: $\sigma_i(D) = \gamma_{th}(x_i^{-1/2})D_i + \gamma_{L_{\text{eff}}}(x_i^{-1/2})D_i$

$\rho_{ij} \equiv$ spatial correlation between gate $i$ and $j$ with separation $d_{ij}$

$$= \begin{cases} 
1 - d_{ij} / X_L(1 - \rho_B) & d_{ij} \leq X_L \\
\rho_B & d_{ij} \geq X_L 
\end{cases}$$

$X_L$ characteristic correlation length
$\rho_B$ characteristic correlation baseline

Large scale model
Simulation Results

- a) Deterministic design objective
- b) Minimize delay variations due to Vth
- c) Min. delay var. due to Vth and L_eff
- d) Min. delay var. due to Vth, L_eff and Spa. Corr.
Simulation Results

- Focus on the last analysis which considers both delay variations due to $V_{th}$ and $L_{eff}$, and spatial correlations

a) Deterministic design
   \[\sigma(D) = 3.02, \text{ yield } = 63\%\]

b) Minimize delay variations due to $V_{th}$
   \[\sigma(D) = 1.96, \text{ yield } = 92\%\]

c) Min. delay var. due to $V_{th}$ and $L_{eff}$
   \[\sigma(D) = 1.52, \text{ yield } = 97\%\]

d) Min. delay var. due to $V_{th}$, $L_{eff}$ and spatial correlation
   \[\sigma(D) = 1.36, \text{ yield } = 98\%\]
MOS Test Structures

• NMOS array equipped to allow full 4-pt probing:
Current Objectives

• Design analytical Monte Carlo simulation framework constructed using macromodels

• Investigate effects of spatial variation (based on historical study) on circuit performance variability using analytical Monte Carlo framework

• Deploy new test structures to explore mid-range (10-1000 micron) spatial variability

• Submit additional test structures for manufacture; gather measurements from fabricated test structures

Future Goals

• 9/1/06: Submit novel ELM and MOS test structures to foundry.
• 10/1/06: Begin measurement/analysis of second round of CD-only test structures.
• 1/1/07: Incorporate CD measurements into Monte Carlo framework.
• Spring, 2007: Refine simulation results with updated CD variation/correlation information;
• Receive and begin measurements on MOS test structures.
Future Projects

• **Line Edge Roughness.** In the sub-42nm nodes LER is gaining prominence in at least two different operating regimes.
  - In the full-on saturation regime, minimal width devices suffer increased channel length variability due to LER. This, of course, complicates our understanding of critical path performance.
  - In addition, in the “off” regime, we experience leakage currents exponentially dependent on the actual channel length. Again, LER adds a complex variability component that must be understood and controlled.

• Create a comprehensive statistical variability model where LER is captured in conjunction with the long distance large scale variability of CDs, and its impact in the saturation and the off regimes is characterized by means of state of the art device simulation.

• **Model- Based Integrated OPC.** Accelerate OPC computations using sensitivity models for the lithography process, and to extend OPC to post-etch and post-planarization pattern transfer.
  - Capture the effect of making small perturbations in the mask layout on printed features. Sensitivity models can be constructed experimentally using special masks with test structures, or through simulation (though simulation techniques are limited to post-develop pattern transfer).
  - Construct a library of image primitives, and to determine sensitivity models for these primitives. OPC calculations are conducted off-line for these primitives. Then, a given mask file is decomposed into primitive elements. Our pre-computed corrections are valid in the interior of each primitive.

• Conduct OPC computations on the boundaries of the primitive elements, and on portions of the mask file that are not part of any primitive library element.

• **Vertically integrated OPC.** All conventional OPC methods begin with a mask tape-out in GDSII or OASIS format, and calculate appropriate corrections to the mask layout to optimize the printed pattern.
  - These methods ignore the structure of the input mask file. Indeed, this file is not a random binary image, but is constructed from standard cell library elements which are optimally positioned (with respect to power and switching speed) by a placement optimizer.
  - The central idea of this project is to exploit this prior information in accelerating OPC computations. Mask corrections for standard cell library elements can be leisurely computed off-line. These are valid only in the interior of the library element because of edge loading effects.

• What remains is to calculate mask corrections at the boundaries of the standard cells. This can be done using standard rule-based or model-based OPC methods. If existing OPC algorithms run in O(n) time, our technique require only (approximately) O(n½)
Proposed Milestones (Year IV)

• Existing 4th year Milestones
  – Final phase of CD uniformity control project. This is done one year early, so it is no longer needed.
  – Complete study of Feed-forward and feedback based schemes for process/equipment control to enhance feature level pattern transfer. Study various control architectures in terms of sensor integration, implementation cost, and expected benefit. No longer relevant in this form.
  – Real time feature-level test structures. This continues, but it is now being picked up by the SRC-funded project.
  – Develop feature-level test structures that can be monitored for real-time insight in their evolution. Examples include real-time etch-rate monitors that are subject to micro loading. No longer relevant.

• New 4th year Milestones
  – Complete Aerial image Sensor Testing Phase. Interact with key company collaborators for testing beyond the UC Berkeley Microlab.
  – Incorporate LER into the process variability problem
  – Complete initial feasibility study of our Model-based OPC approach on a small-scale mask file.
  – Develop algorithms to search for library cells in mask files, and to determine cell boundaries. Trial run of vertically integrated OPC on a simple mask.