Motivation

- Spatial correlation and decomposition of CD variation have been treated separately & incompletely
- We wish to merge the two concepts into one cohesive model with spatial dependency
- Apply this accurate model in a Monte Carlo simulation framework
- Use MC framework to investigate:
  - Design techniques to reduce sensitivity to CD variation
  - Process control approaches to reduce CD variation

Specific focus of this work: detailed analysis of spatial variation in gate length in the 0.2µm to 1.15mm separation distance range

Decomposition of Spatial CD Variation

- Average Wafer
- Scaled Mask Errors
- Within-Field Variation
- Across-Wafer Variation

Autocorrelation in Random Variation

- “Random” variation has slight correlation structure at short end of separation distance range
- \( mm \)-scale spatial correlation is accounted for by systematic variation.
- \( \mu m \)-scale correlation may still have structure

Raw Data (Averaged Across Chips)

- 25 total pre-diced chips (wafer location unknown)
- Two instances per chip (horiz, vert), 9 DUT’s per chip, 17 measurement positions within each DUT
- 3825 total measurements for each orientation

Pattern Density-Dependent Etch Model

- Etch microloading can explain the deterministic pattern observable in measurements from DUT’s 1-4
- Model contains two density metrics
  1) “Local” density: intended to capture shorter-range etch effects, we count the total polysilicon area within a moving window that is centered on the line in question
  2) “Global” density: intended to capture longer-range etch effects, we calculate the total area of polysilicon within a given DUT
- Both terms statistically significant (\( p<0.0001 \)) in model fit using LSR

Breakdown of \( \mu m \)-Scale Variance

- Etch microloading model accounts for roughly 1/3rd of the \( \mu m \)-range spatial variation
- Does autocorrelation exist in the remaining residuals?

Ongoing Test Structure Design

- Novel test structures for decoupling CD variation from other sources of device parameter variation (mainly \( V_{th} \))
- Interleave two test structures on a single chip
  1) \( D_1 \)
  2) MOS electrical performance test structures
- Decouple spatial CD signature from fingerprint of full MOS electrical variation

MOS Array Design

- NMOS array equipped to allow full 4-pt probing

Summary

- Measurement & analysis of short-range ELM test structures is complete
  - After modeling pattern-dependent variation, spatial correlation in residuals is negligible
- Ongoing work in broadening understanding of spatial variation to other device parameters and general electrical performance