

Steven L. Moran

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Objective

Study and develop new technologies for IC design such as integrating dies on a silicon interconnect fabric and utilizing maskless lithography.

Education

University of California, Los Angeles, 2012-2021 (expected)

Ph.D. in Electrical Engineering, Circuits & Embedded Systems, 2021 (expected)

M.S. Electrical Engineering, Circuits & Embedded Systems, 2017 (expected)

B.S. in Electrical Engineering with honors, Integrated Circuits, 2016

Awards/Honors

- UCLA Electrical Engineering Departmental Fellowship, 2016
- UCLA Engineering Kalosworks.org Scholarship, 2016
- IEEE Power & Engineering Society Scholar, 2015
- UCLA Engineering Berman Family Undergraduate Scholarship Endowment, 2014 & 2015
- UCLA Engineering John Richard Leffler Undergraduate Scholarship, 2013

Research Interests

- Interconnect Fabrics
- Integrating dielets near on-chip wiring levels
- Maskless Lithography
- Neuromorphic Computing

Technical Skills

Experience with Cadence (Spice), C/C++, Linux, Matlab, Simulink, etc.

Work Experience

Reliability Engineering Intern – Space Systems Loral (SSL)

June 2014 – September 2015 (4 months)

- Studied the On-orbit Fleet Reliability of SSL-built satellites
- Performed analysis on payload sparing and spare consumption throughout the lifetime of a satellite
- Analyzed the on-orbit FIT (failure-in-time) rate of Transmitting Wave Tube Amplifiers
- Analyzed how part and unit failures on spacecraft occur over time

IC Test Engineering Intern – Finisar Corporation

June 2014 – August 2014 (3 months)

- Learned about the manufacturing and testing process of wafers and IC's
- Helped test and provided analysis for several Laser Driver and Post-Amplifier IC's for fiberoptic modules
- Analyzed wafer sort, IV-curve, package qualification, HTOL, ATE, output impedance, and other types of data

Groups & Associations

UCLA IEEE | Engineering Society of UCLA | UCLA HKN Honor Society | UCLA UPE Honor Society
UCLA Alumni Scholars Club | UCLA BEAM (Building Engineers and Mentors)