Hye In Lee

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Objective

To find an internship position in the digital VLSI design methodology area

Research Interests

- ✓ Design methodology for low power and high performance VLSI circuits
- ✓ Resilient and reliable system and design, design for stress

Education

University of California, San Diego, La Jolla, CA

Ph.D student in Dept. of Electrical Computer Engineering — 09/2012- present
(Advisor: Prof. Andrew B. Kahng)

- ✓ Research Area: Physical design, Design-manufacturing-interface

Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea

M.S. in Dept. of Electrical Engineering (Advisor: Prof. Youngsoo Shin) — 02/2007 - 01/2009

- ✓ Selected Courses: Computer Aided Design of VLSI Circuit and Systems, Digital Integrated Circuit, Computer Architecture, Design and Analysis of Algorithm, Electronics Lab., System Programming
- ✓ Research Area: Sequential Circuit Optimization using Pulsed Latch(M.S. thesis)

Yonsei University, Seoul, Korea

B.S. in Dept. of Electrical Engineering — 03/2003 - 02/2007

Employment

Samsung Electronics System LSI Division

Research Engineer in Design Technology Team — 02/2009 -08/2012

- ✓ Developed statistical leakage power analysis methodology considering process variability — 06/2009 - 08/2012
- ✓ Researched on variation-tolerant design methodology — 02/2010 - 08/2012
- ✓ Provided technical supports for top-tier customers — 03/2011 - 08/2012

Publications

Journal Paper

- ✓ **Hyein Lee**, Seungwhun Paik, and Youngsoo Shin, "Pulse Width Allocation and Clock Skew Scheduling: Optimizing Sequential Circuits based on Pulsed Latches," Institute of Electrical and Electronics Engineers (IEEE) Transaction on Computer-Aided Design of Integrated Circuits and System (TCAD), vol. 29, no. 3, pp. 355-366, Mar. 2010. **(Top 25 downloaded articles for IEEE TCAD in 2010)**

Conference Paper

- ✓ A. B. Kahng, S. Kang and **H. Lee**, "Smart Non-Default Routing for Clock Power Reduction", Proc. Design Automation Conference, 2013, to appear.
- ✓ Kyung-Tae Do, Jung Yun Choi, Seokhoon Kim, **Hyein Lee**, Hyo-Sig Won, Kyu-Myung Choi, "A Practical Framework for Statistical Leakage Estimation," Design Automation Conference (DAC) User Track, Jun. 2010.
- ✓ **Hyein Lee**, Seungwhun Paik, and Youngsoo Shin, "Pulse Width Allocation with Clock Skew Scheduling for Optimizing Pulsed Latch-based Sequential Circuits," International Conference on Computer-Aided Design (ICCAD), Nov. 2008.

Patent

- ✓ **Hyein Lee**, Seungwhun Paik, and Youngsoo Shin, "METHOD AND APPARATUS FOR IMPROVING SPEED OF PULSED LATCH-BASED DIGITAL SEQUENTIAL CIRCUITS," Korea patent 10-0989899, Oct. 2010.

Skills

- ✓ Programming Languages: C/C++(with MFC), Verilog, TCL, Python, Java
- ✓ Design Tools: NC-Verilog, Design Compiler, IC Compiler, PrimeTime, StarRCXT, Calibre, Virtuoso, HSPICE, FineSim-SPICE, HSIM
- ✓ Math/Statistic Tools: MATLAB, Minitab
- ✓ Language: Korean(native), English(fluent), and French(beginning level)

Reference is available upon request.