LUTONG WANG

Ph.D. Student, Electrical and Computer Engineering Department, University of California at San Diego

CONTACT

Address: EBU3B Room 2144,
9500 Gilman Drive #0404, UC San Diego, La Jolla, CA 92093 E-mail: luw002@ucsd.edu

EDUCATION

University of California, San Diego, CA *09/2014 – Present*
Ph.D. in Department of Computer Science and Engineering
GPA: 3.9/4.0

University of California, San Diego, CA *09/2014 – 06/2016*
M.S. in Electrical and Computer Engineering

Tsinghua University, Beijing, China *09/2010 – 07/2014*
B.S. in Microelectronics

RESEARCH EXPERIENCE

Improved Physical Design for Placement Optimization *UC San Diego*
- RePlAce: Improved Solution Quality and Validation of Routable Placements
- Optimal Multi-Row Detailed Placement for Yield and Model-Hardware Correlation Improvements [C5]
- Vertical M1 Routing-Aware Detailed Placement for Congestion and Wirelength Reduction [C4]

Improved Physical Design for Low Power Optimization *UC San Diego*
- Improved Flop Tray-Based Design Implementation for Power Reduction [C2]

DFM Methodologies for Advanced Nodes *UC San Diego*
- ILP-Based Co-Optimization of Cut-Mask Layout, Dummy Fill and Timing for Sub-14nm BEOL Technology [C1]
- MILP-Based Optimization of 2D Block Masks for Timing-Aware Dummy Segment Removal in Self-Aligned Multiple Patterning Layouts [J1]

PUBLICATIONS (AUTHORS ARE ALPHABETICALLY ORDERED)

[J1] K. Han, A. B. Kahng, H. Lee and **L. Wang**, "MILP-Based Optimization of 2D Block Masks for Timing-Aware Dummy Segment Removal in Self-Aligned Multiple Patterning Layouts", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 36(7) (2017), pp. 1075-1088.

[C5] C. Han, K. Han, A. B. Kahng, H, Lee, **L. Wang** and B. Xu, "Optimal Multi-Row Detailed Placement for Yield and Model-Hardware Correlation Improvements in Sub-10nm VLSI", *IEEE/ACM International Conference on Computer-Aided Design*, 2017, to appear.

[C4] K. Han, A. B. Kahng, H. Lee and **L. Wang**, "Vertical M1 Routing-Aware Detailed Placement for Congestion and Wirelength Reduction in Sub-10nm Nodes", *ACM/EDAC/IEEE Design Automation Conference, 2017*, pp 51:1-51:6.

[C3] K. Han, A. B. Kahng, H. Lee and **L. Wang**, "Performance- and Energy-Aware Optimization of BEOL Interconnect Stack Geometry in Advanced Technology Nodes", *IEEE International Symposium on Quality Electronic Design*, 2017, pp. 104-110. (**Invited Paper**)

[C2] A. B. Kahng, J. Li and **L. Wang**, "Improved Flop Tray-Based Design Implementation for Power Reduction", *IEEE/ACM International Conference on Computer-Aided Design*, 2016, pp. 20:1-20:8. (nominated for **Best Paper award**)

[C1] K. Han, A. B. Kahng, H. Lee and **L. Wang**, "ILP-Based Co-Optimization of Cut-Mask Layout, Dummy Fill and Timing for Sub-14nm BEOL Technology", *SPIE Photomask Technology*, 2015, pp. 96350E. (nominated for **Best Paper award**)

SKILLS

[*Languages*] C/C++, Tk/Tcl, Python, Matlab, Verilog
[*Tools*] SoC Encounter / Innovus / ICC, Tempus / PrimeTime, Design Compiler, Quantus / Star-RCXT, HSPICE, CPLEX
[*Others*] LaTex, Word, Excel, PowerPoint