
LUTONG WANG

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EDUCATION

University of California, San Diego	Sept. 2014 – present
• M.S. in Computer Engineering	Current GPA: 3.93/4.00
Tsinghua University, Beijing	Sept. 2010 – July 2014
• B.Eng. in Microelectronics	

RELATED COURSEWORK

VLSI Digital System Algorithms & Arch (A+)	Intro to Synthesis Method in VLSI CAD (A+)
VLSI Integrated Circuits & System Design (A+)	Intro to Embedded Computing (A+)
VLSI Advanced Topics	Algorithm Design and Analysis (A+)
Algorithm & Optimization in VLSI CAD	Principles of Computer Architecture

SKILLS

Tools: Cadence EDI, Synopsys DC / ICC / PrimeTime, IBM CPLEX, Hspice
Programming languages: C/C++, Verilog, TCL, MATLAB, ModelSim, Xilinx ISE
Languages: English, Chinese

RESEARCH

Cut Mask Optimization	Mar. 2015 – present
• Co-optimization of timing with design rules consideration	
• Exploring trade-offs of performance and cost in sub-14nm backend-of-line (BEOL) technology	
International Technology Roadmap for Semiconductors (ITRS)	June 2015 – present
• System integration analysis of smartphone, smart object and cloud services	

PUBLICATION

K. Han, A. B. Kahng, H. Lee and L. Wang, "**ILP-Based Co-Optimization of Cut Mask Layout, Dummy Fill and Timing for Sub-14nm BEOL Technology**", *Proc. 36th BACUS Symposium on Photomask Technology and Management*, 2015.

PROJECTS

<i>EM-Aware Multi-Mode Physical Implementation</i>	Mar. 2015
• Nominal and overdrive EM-aware signoff (1 st place among 27 groups)	
<i>Leakage Power Minimization</i>	Feb. 2015
• Sensitivity guided cell swapping and gate sizing (1 st place among 27 groups)	
<i>Design, Implementation and Optimization of FFT IP</i>	Jan. 2015
• Multi-cycle design with customized multiplier implementation (1 st place among 27 groups)	
<i>Design, Layout and Optimization of a Single-Cycle Microprocessor</i>	Dec. 2014
• High energy efficiency operating in sub-threshold region with clock/power gating	

AWARDS & HONORS

Zheng Geru Scholarship, Tsinghua University (top 10% GPA)	2013
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