Kwangsoo Han

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Contact

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Research Interests

Management of Variability in VLSI Design (Clock Tree Optimization)

Design for Manufacturability (Optimization and Mathematical modeling)

Education

University of California, San Diego, La Jolla, CA **Sep.2013 - Present**

- PHD student in Electrical and Computer Engineering
- Advisor: Andrew B. Kahng (VLSI CAD Laboratory)

Hanyang University, Seoul, South Korea **Mar.2011 - Feb.2013**

- M.S. in Electrical and Computer Engineering (4.38/4.5)
- Advisor: Ki-Seok Chung (Embedded System on Chip Laboratory)

Hanyang University, Seoul, South Korea **Mar.2005 - Feb.2011**

- B.S. in Media Communication Engineering (4.21/4.5)
- Summa cum laude honor

Research Experience

Benchmarking of Mask Fracturing Solutions **Nov.2013 - Present**

- Estimate lower bound and find optimal solution
- Construct optimal benchmarks of mask fracturing solution

Development of Configurable Device & SW Environment **Dec.2011 - Jun.2012**

- Design a slice-level configurable device of FPGA
- Characterize the timing of slice and make a cell library

Reed Solomon module for high-density and multiple data processing **Mar.2011 - Nov.2011**

- Design an Error Correcting Code (ECC) communication chip based on Reed Solomon algorithm
- Tape out an ECC communication chip in November 2011

Publications

- T.-B. Chan, **K. Han**, A. B. Kahng, J.-G. Lee and S. Nath, "OCV-Aware Top-Level Clock Tree Optimization", Proc. Great Lakes Symposium on VLSI, 2014, to appear
- D. Jeon, **K. Han** and K. Chung, “A Robust Level Shifter Design for Improving Performance of Mobile Device”, IEEE International Conference on Consumer Electronics (ICCE), 2013
- **K. Han**, D. Jeon and K. Chung, “Ultra Low Power and High Speed FPGA Design with CNFET”, International Symposium on Communications and Information Technologies (ISCIT), 2012
- **K. Han**, D. Jeon and K. Chung, “Low Power and High Speed Level Shifter with CNFET”, International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), 2012
- D. Jeon, **K. Han** and K. Chung, “A High Performance Low Power Level-up Shifter Design for Dual Supply Volatages”, International Technical Conference on Circuits/Systems, Computers and Communications (ITC-CSCC), 2012
- **K. Han**, D. Jeon and K. Chung, “Dual Step Level Shifter”, Korea Patent No.10-2012-0114726, 2012

Key Skills

Proficient or familiar with a vast array of programming languages and design tools.

C/C++, JavaScript Tcl	Design Complier, HSPICE Prime Time	Encounter, Virtuoso Calibre DRC/LVS	Modelsim, MATLAB VHDL, Verilog