Wei-Che Wang

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EDUCATION

2013.8 ~ Present **University of California, Los Angeles**

Ph.D in Electronics Engineering

- GPA: 3.7

2007.9 ~ 2009.6 **National Taiwan University**

M.S. in Electronics Engineering

- GPA: 4.0
- Awards:
  - NTU GIEE Technical English Presentation 3rd Place
  - ACM CADathlon at ICCAD Selection 8th Place
- Selected Academic Projects:
  - Thesis: Test Response Compaction In The Presence Of Many Unknowns
  - National Science Council HOY Project: Wireless VLSI Testing System
  - LFSR-Based Encoder Engine
  - Displacement Minimization for Legalization in Standard Cell Placement

2003.9 ~ 2007.6 **National Taiwan University**

B.S. in Computer Science and Information Engineering

- GPA: Overall/Last 2 Years 3.6/4.0
- Academic Project
  - Motion Detection and Pattern Recognition on Moving Objects

WORKING EXPERIENCE

2009.11 ~ 2013.07 **Taiwan Semiconductor Manufacturing Company Limited (TSMC, Taiwan)**

Engineer, Standard Cell Library Department, Design Technology Division

- Award:
  - 2012/Q3 Design Technology Platform Customer Service Award Nomination
- Selected Projects:
  - Efficient Look-Up-Table Design Automation of N28/N20 Standard Cell Library
  - Quality Checking Flow Design on Cell MPW, Vccmin, and Multi-Bit DFF Behavior Verification

- N16 FinFet Characterization Flow Development
- Customization Coarse-Grain RSDF Circuit Design

2011.08 ~ 2012.01 **Advanced Micro Devices (AMD, San Jose, CA) On-Site GPU Project Support**

TEST SCORES

2012.4	**TOEFL**	**Total 112** (R29/ L27/ S29/ W27)
2011.4	**GRE**	**Total 1500** (V700/ Q800/ AWA 3.5)

RESEARCH INTERESTS

- Electronic Design Automation on Novel devices/Packaging/Testing
- VLSI on Low Power, High Performance SOC system design and analysis

PUBLICATIONS

[1] W.-C. Wang, C.-Y. Hsu, J. C.-M. Li, Y.-C. Sung, A. Rao, and L.-T. Wang, "Row-Linear Feedback Shift Register-Column X-Masking Technique for Simultaneous Testing of Many-Core System Chips," *IET Computers & Digital Techniques*, Volume 5, Issue 4, pp. 238-246, 2011.

[2] W.-C. Wang, C.-Y. Hsu, J. C.-M. Li, Y.-C. Sung, A. Rao, and L.-T. Wang, "Row-LFSR-Column (RLC) Test Response Masking Technique," *VLSI/CAD Symposium*, 2010.

[3] W.-C. Wang, C.-Y. Hsu, and J. C.-M. Li, "Test Response Compact in the Presence of Many Unknowns," *VLSI Test Technology Workshop*, 2009.

[4] F.-M. Wang, W.-C. Wang, and J. C.-M. Li, "Time-Space Test Response Compaction and Diagnosis Based on BCH Codes," *IET Computers & Digital Techniques*, Volume 3, Issue 3, pp. 304-313, May 2009.