

# YASMINE AHMED BADR

11737 Darlington Avenue, Apt 105  
Los Angeles, CA 90049  
U.S.A

Email : [ybadr@ucla.edu](mailto:ybadr@ucla.edu)  
Cellular: +1 (310) 913- 4683

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## EDUCATION

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- Ph.D.** Fall 2012- present  
NanoCAD lab <http://nanocad.ee.ucla.edu>  
Electrical Engineering Dept,  
University of California, Los Angeles (UCLA)  
Current GPA: 3.9
- M.Sc.** 2012  
Computer Engineering Dept.  
Cairo University  
*GPA in Pre-master courses:* 3.856  
*Thesis Title:* Automated Layout Retargeting for Self- Aligned Double Patterning Decomposability
- B.Sc.** 2009  
Computer Engineering Dept.  
Cairo University  
*Total grade:* Distinction with Honors  
*Rank:* 3<sup>rd</sup>  
*Graduation Project: **Split-It!***: A Layout Splitting Algorithm for *Double Patterning Photolithography*  
*Graduation Project Grade:* Distinction
- High School Certificate** 2004  
Ramses College For Girls  
*Results:* 99% + 1% High Level

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## WORK EXPERIENCE

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- Summer Graduate Intern July 2014-September 2014  
Design to Silicon Division,  
*Mentor Graphics*, OR, U.S. <http://www.mentor.com>
  - Worked on Directed Self Assembly (DSA) and its integration with Multiple Patterning (MP) in Calibre tool
- Teaching Assistant September 2009- August 2012  
Computer Engineering Dept.  
*Cairo University*, Egypt <http://ww.eng.cu.edu.eg>
  - Tutored in Computer Architecture, Digital Design, Modeling & Simulation, Software Testing, Software Engineering, Database Systems, Advanced Programming Techniques and Networks courses, in addition to Operating Systems and Microprocessors labs
- Part-time Software Development Engineer November 2010- July 2012  
Chameleon ART team  
*Mentor Graphics*, Egypt <http://www.mentor.com>
  - Worked on Layout Migration Engine. Job duties included research to enhance the optimization

engine and add new features to the tool.

Research Assistant (Graduate Intern)

May 2010- October 2010

Microsoft Advanced Technology Labs, Egypt <http://research.microsoft.com/en-us/labs/atlc/default.aspx>

– Conducted research in Object Detection, Computer Vision

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## PUBLICATIONS

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- **Badr, Y.**; Torres, A.; Gupta, P.; “Mask Assignment and Synthesis of DSA-MP Hybrid Lithography for sub-7nm Contacts/Vias”; *Design Automation Conference*, 2015
- **Badr, Y.**; Torres, A.; Gupta, P.; “Incorporating DSA in multi-patterning semiconductor manufacturing technologies”; *SPIE Advanced Lithography*, 2015
- Ghaida, R.; **Badr, Y.**; Gupta, P.; “Pattern-restricted design at 10nm and beyond,” in *Proc. IEEE International Conference on Computer Design*, 2014 [Invited Paper]
- **Badr, Y.**; Ma, K.-w.; Gupta, P.; “Layout pattern-driven design rule evaluation,” *SPIE Journal of Micro/Nanolithography, MEMS and MOEMS (JM3)*, 2014
- **Badr, Y.**; Ma, K.-w. Ma; Gupta, P.; Pattern-drive Design Rule Evaluation; *SPIE Advanced Lithography*, 2014
- Ghaida, R.; **Badr, Y.**; Gupta, M., Jin, N.; Gupta, P.; Comprehensive Die-Level Assessment of Design Rules and Layouts; *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2014
- **Badr, Y.**; Wassal, A; "Split-It!: From Litho Etch Litho Etch (LELE) to Self-Aligned Double Patterning (SADP) Decomposition"; *SPIE Photomask Technology*; 2012
- Darwish, H.; Shagar, H.; **Badr, Y.**; Arafa, Y.; Wassal, A.; “A Hashing Mechanism for Rule-Based Decomposition in Double Patterning Photolithography”; *22<sup>nd</sup> International Conference on Microelectronics (ICM)*, 2010

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## SELECTED GRADUATE COURSES

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Design for Manufacturing, Electronic Design Automation, Linear Programming, VLSI Design, Matrix Analysis, Computer Architecture

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## SELECTED UNPUBLISHED PROJECTS

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### Graduate Projects:

- *DSA Compatibility Study*: Performed a study of the DSA-compatibility of DSA-unaware layouts
- *Snake Router*: Built a standard cell router. (Rank: 2<sup>nd</sup>)
- *Match-It!*: Developed a Machine-learning based framework for Hot Spot Detection

### Undergraduate Projects:

- *Digital Design and Computer Architecture*: Designed and built, using a Simulation tool, the architecture of a processor with PDP-11 Instruction set
- *Embedded Systems*: Implemented a motor-controlling device, with feedback and In System Programming facility on AT89S51 microcontroller
- *Software Engineering*: Developed a Graph Modeling and Drawing tool in ANSI C++ (engine) and Visual C++.Net (GUI)
- *Pattern Classification*: Developed a Sketch Recognition Software
- *Interfacing*: Implemented a vehicle for painting sports courts according to a given drawing

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## UNDERGRADUATE INTERNSHIPS

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Clausthaler Umwelttechnik-Institut GmbH (CUTECH), Germany

Summer 2008

Modeling and Simulation Department

- Worked, in a Research group, on the simulation of the Visual Cortex, Neural Networks

*Mentor Graphics*, Egypt

Summer 2007

Embedded Systems Development (Volcano team)

- Developed Embedded C code for an HCS12 microcontroller

*IBM*, Egypt

Summer 2007

Software Development group

- Built applications that run on Lotus Notes Clients, using Lotus Domino Designer

*ITWorx*, Egypt

Summer 2006

Technical Architecture group

- Built a high intelligence tool, used for harness assembly in electrical planning, using C#, Oracle Database Client in .Net framework, XML Web Service, ASP.Net & Javascript.

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**SKILLS**

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**Programming Skills**

- OO programming in C++, C#
- Embedded C
- Matlab programming

**Other Technical Skills**

- Digital circuits simulation using Altera, Quartus II and ModelSim
- Verilog
- Working with IC layouts with Mentor Graphics Calibre tool
- Working in Linux (including csh scripting) and Windows environments

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**AWARDS**

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- *Graduate Dean's Scholar Award*, UCLA, 2012-2013
- *Departmental Fellowship* for Ph.D. program in Electrical Engineering; UCLA; 2012
- *TA scholarship* for M.Sc. program in Computer Engineering; Cairo University; 2009 -2012
- *'Dr. Yehia Al-Hakim Award for the Best Graduation Project in Computer Engineering'*; 'Egyptian Engineering Day (EED); IEEE GOLD; 2009
- 1<sup>st</sup> Prize in 'Best Mentor Graphics Sponsored Graduation Project' Contest, 2009
- Ideal student, 2004

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**PROFESSIONAL ASSOCIATIONS**

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Member of IEEE

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**REFERENCES**

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Furnished upon request