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Tackling Electrical Variability in Advanced CMOS Technologies

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IMPACT Webinar, May 15, 2009, UC Berkeley

Outline

- Introduction
- Modeling Considerations
- Tackling Variability
- Summary

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Outline

- Introduction
  - Proximity effects : litho, stress, Vth
- Modeling Considerations
- Tackling Variability
- Summary

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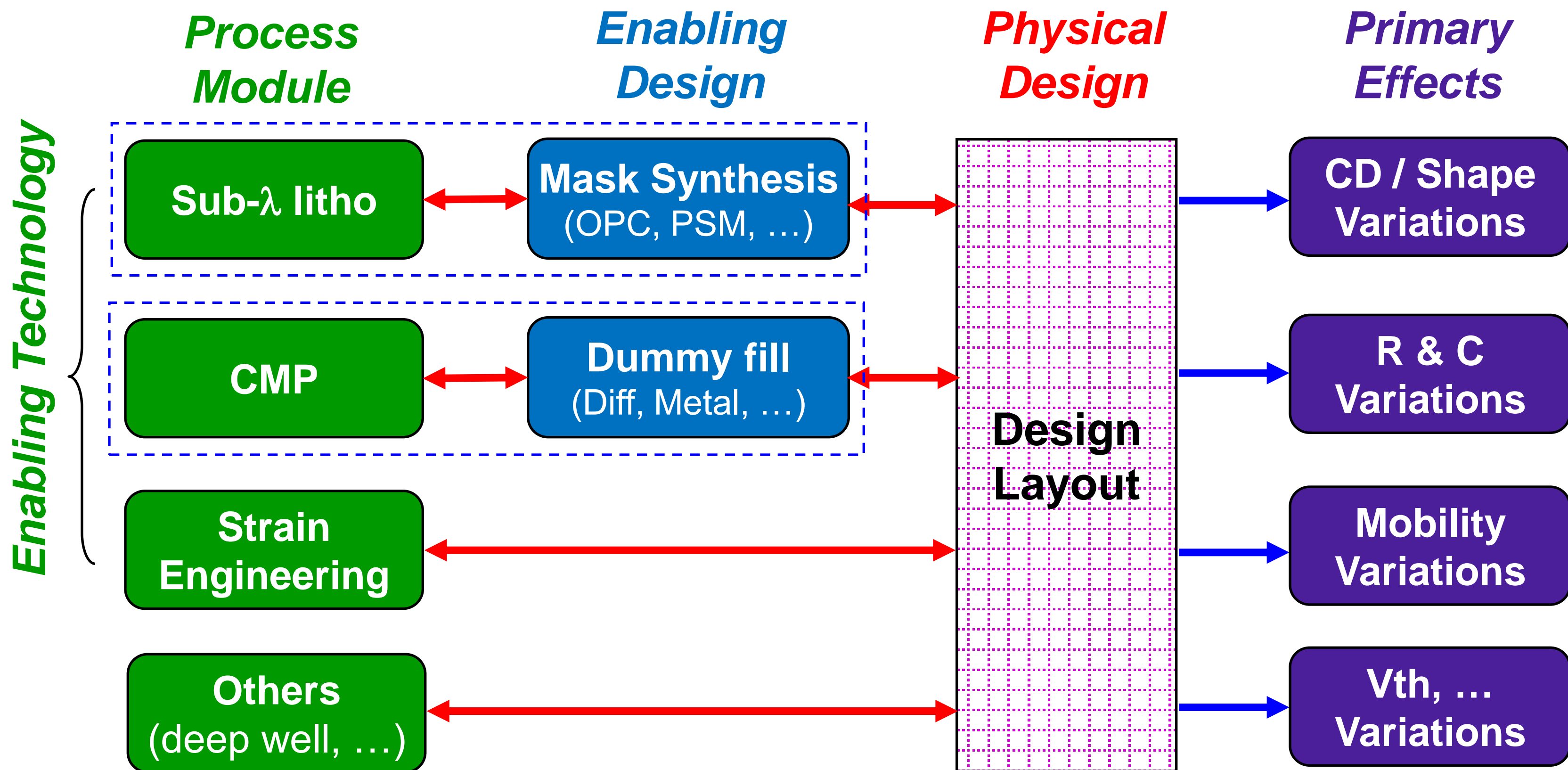
Process and Layout Interactions



- Systematic, layout dependent variations result from process and layout interactions.
- The enabling manufacturing processes are inherently coupled with design.

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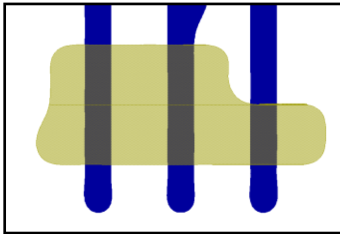
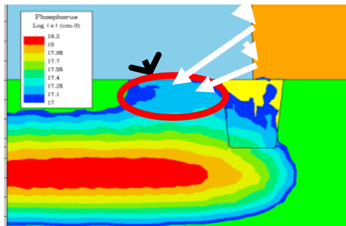
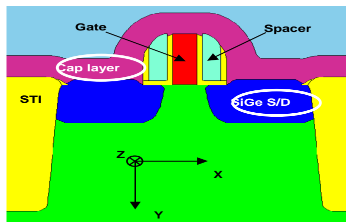
Sources of Layout Proximity Variations



Lithographic Proximity : Poly and Diffusion



Well Proximity (WPE), transient -enhanced diffusion (TED), …



Mechanical stress due to STI, SiGe, ESL, SMT, …

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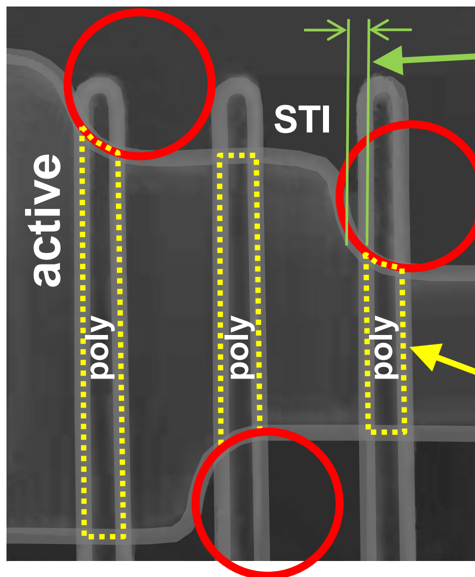
Corner Rounding Gets Worse

- **Different W's require jogs in diffusion mask**



Overlay error (misalignment) aggravates the channel distortion.

The jogs have a fixed curvature radius of ~60nm that can not be improved by OPC. Meanwhile, the poly pitch shrinks by 0.7x with each technology node

The channel shapes become distorted

Max variation at 45nm :
L ~ 5%
W ~ 10%

- ***How does it affect transistor performance?***
  - **Poly gate shape – distorted channel length**
  - **Active layer shape – varied channel width**

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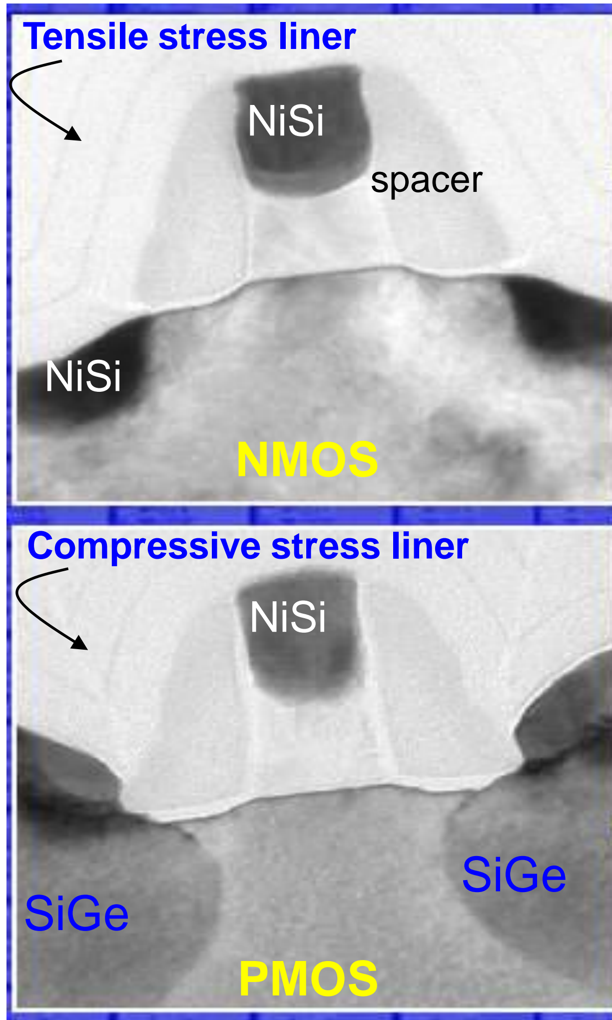
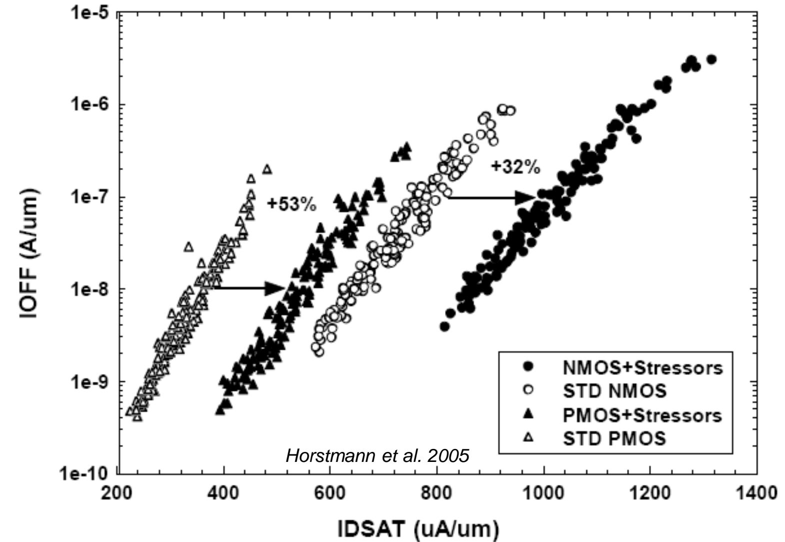
Strain Engineering



An enabling technology since 90nm



- Stress sources:
  - **Stress liner (ESL) : single or dual**
  - **Embedded SiGe (S/D)**
  - **Stress memorization technique**
  - **Strain-Si/SiGe**
  - **Trench contacts**
  - **STI**

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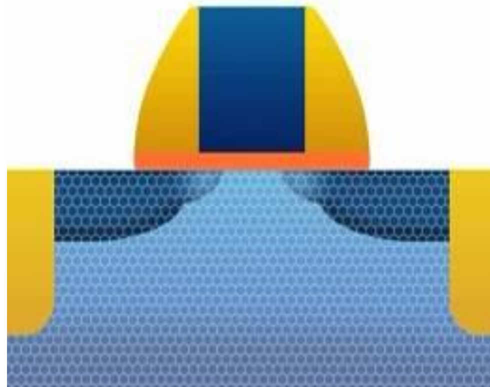
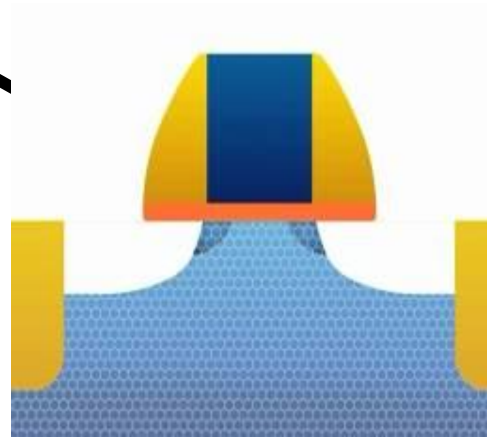
Embedded SiGe Process for PMOS

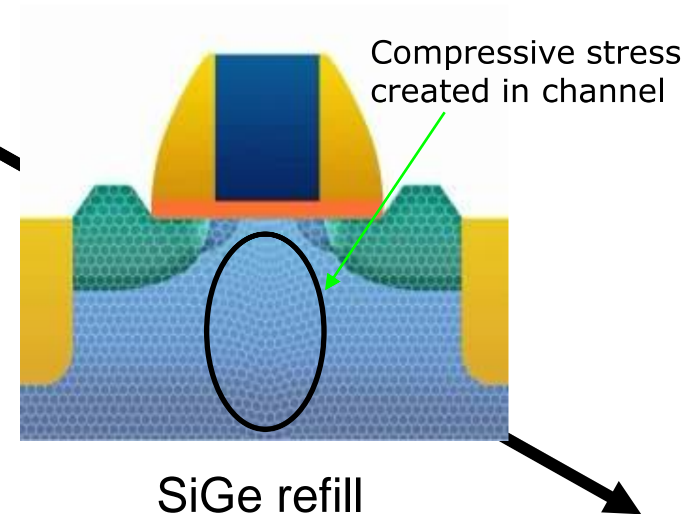


Standard Source/Drain



Source/Drain Etch

Lattice constant:
- *Silicon: 5.43 Å*
- *Germanium: 5.66 Å*
- *$Si_{1-x}Ge_x$: in-between*



SiGe refill

- Si_xGe_{1-x} deposited on Si will adapt to Si lattice (large squeezed to small), leading to compressive misfit stress (uni-axial).

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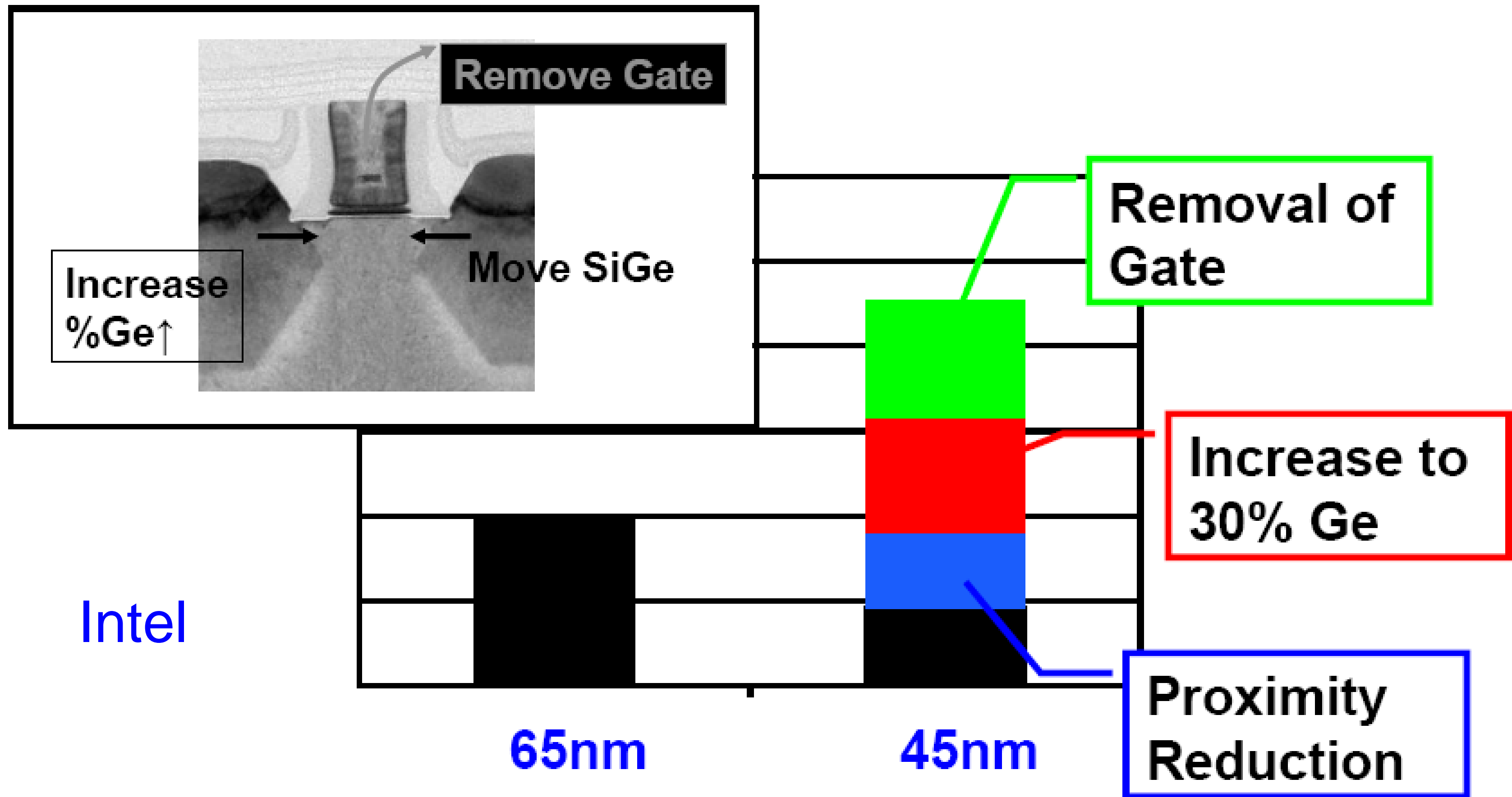
PMOS Enhancements



C. Auth et al. (Intel), VLSI Symposium 2008
K. Kuhn 2009 CMOS Variation Conference (Landon)

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Stress Boost due to Gate Replacement

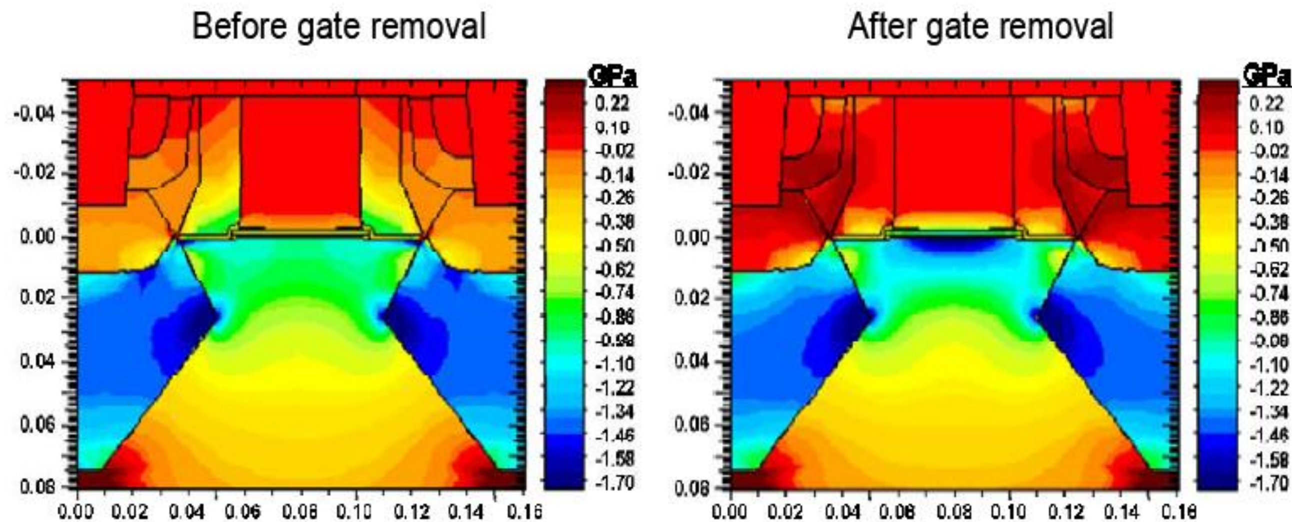

Fig.3 Stress contours in the PMOS transistor before and after the removal of the polysilicon dummy gate. Stress in the channel is shown to increase 50% from ~0.8GPa to >1.2 GPa.

C. Auth et al. (Intel), VLSI Symposium 2008

45nm HK/MG

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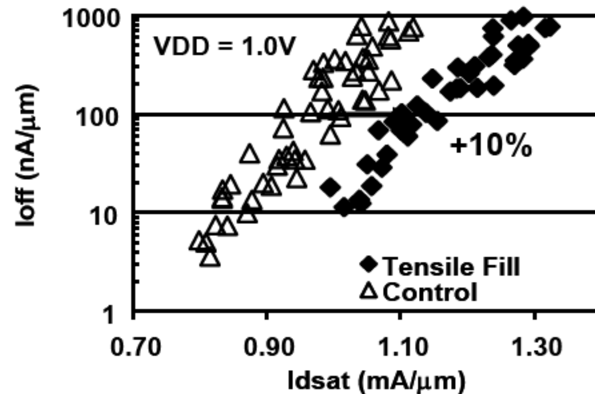
Contact and Gate Induced Stress

- NMOS Enhancement (45nm HK/MG)



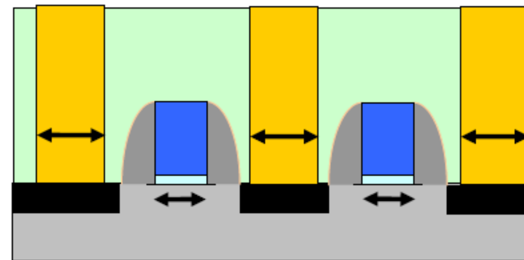
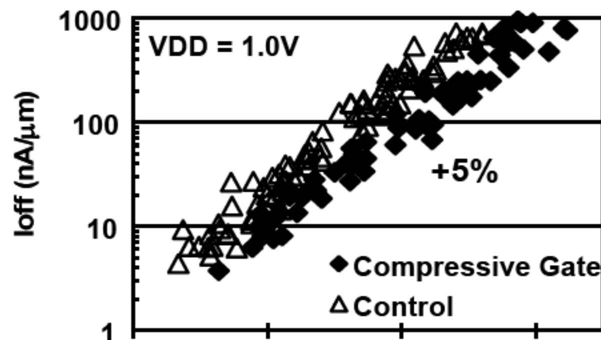


Fig.4 Ion-Ioff benefit of tensile Contact Fill showing a 10% NMOS Idsat benefit. Contact resistance is matched for the two fill materials.



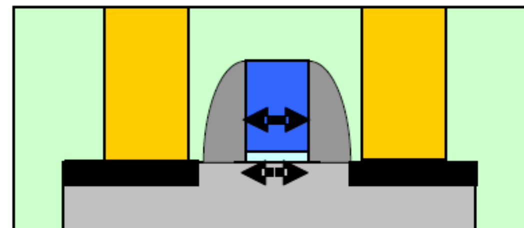


Fig.5 Ion-Ioff benefit of compressive gate stress showing a 6% NMOS Idsat gain. Tensile Contact Fill is used on both sets of data.

C. Auth et al. (Intel), VLSI Symposium 2008
K. Kuhn 2009 CMOS Variation Conference (Landon)

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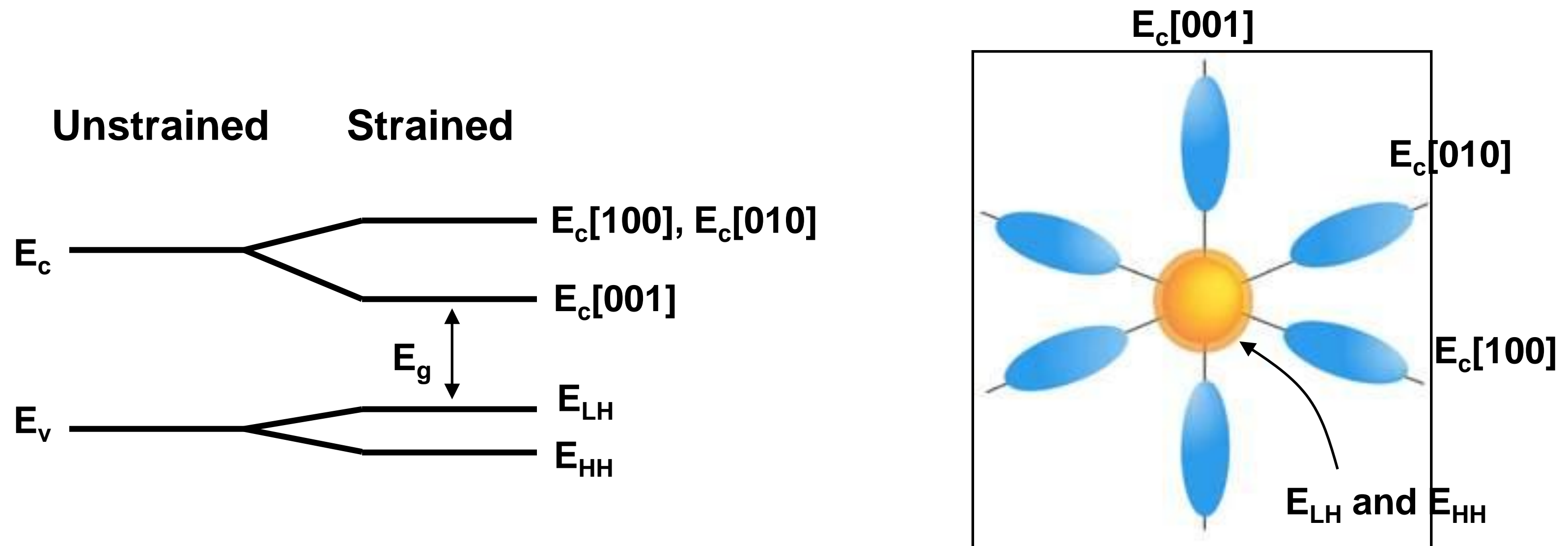
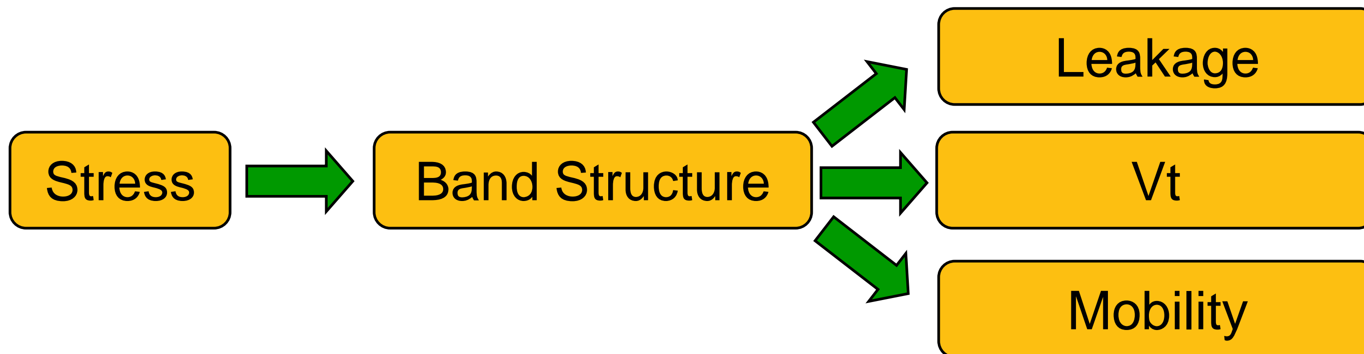
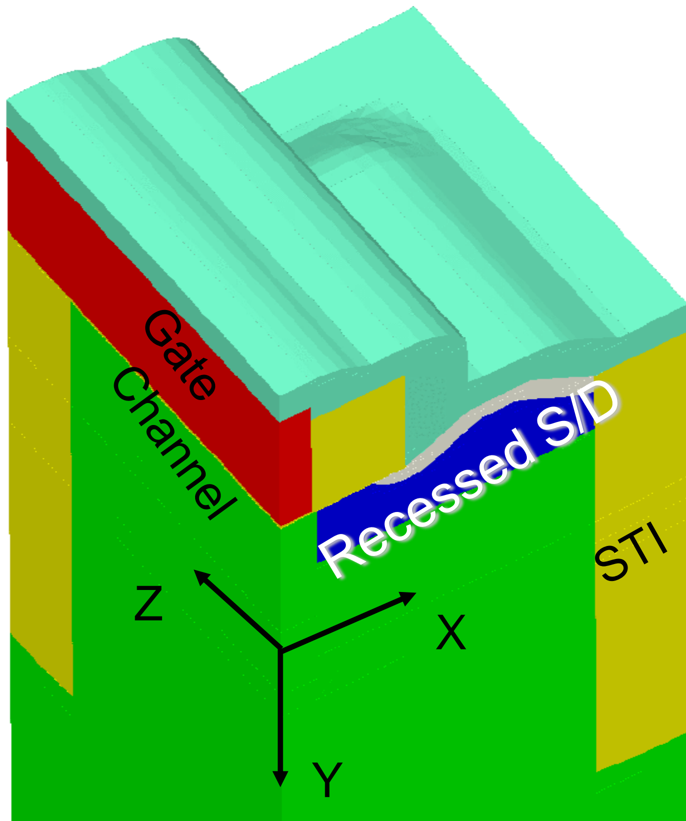
Stress Impact on Band Structure





Complexity of Stress Effects on Mobility



- Direction
- Sense
- Type

Electron and hole mobility change per 1 GPa stress, based on piezoresistance effect

Stress component	Tensile		Compressive	
	nMOS	pMOS	nMOS	pMOS
1 GPa along channel (X) Longitudinal	+30%	-70%	-30%	+70%
1 GPa across channel (Z), Transverse	+20%	+70%	-20%	-70%
1 GPa vertical (Y) Out of plane	-50%	+1%	+50%	-1%

Wafer orientation: (100)/<110>

$$\frac{\Delta\mu}{\mu} \approx \left|\pi_{11}\sigma_{11} + \pi_{\perp}\sigma_{\perp}\right|$$

Piezoresistance coefficients are valid under small and moderate stress, where the piezoresistance varies linearly with stress.

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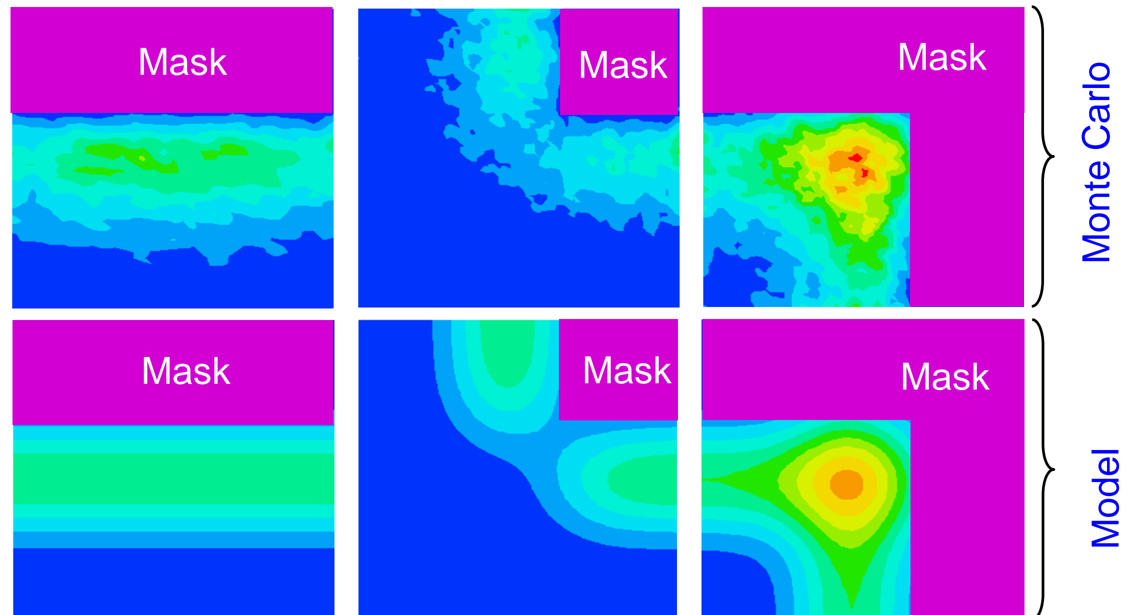
WPE

Instance parameters:
DELVTO, DELK2



- Use more fundamental equations
  - More accurate and predictable
- The model computation is integrated with a dedicated geometry engine for performance, capacity, and efficiency
- Simpler instance parameter set

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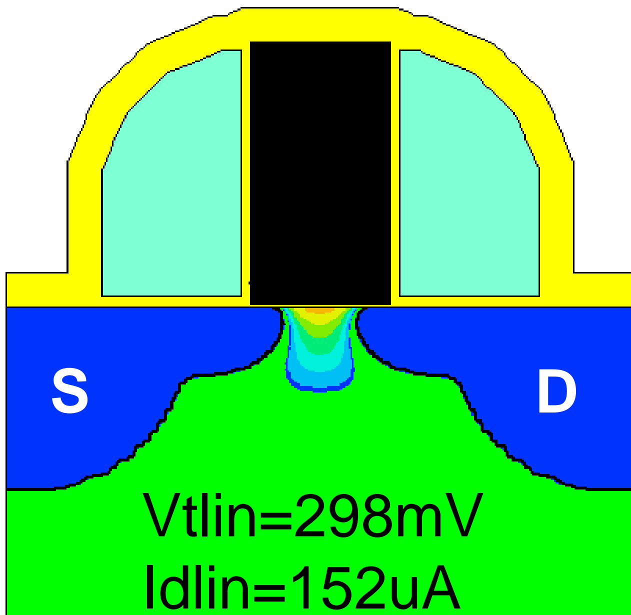
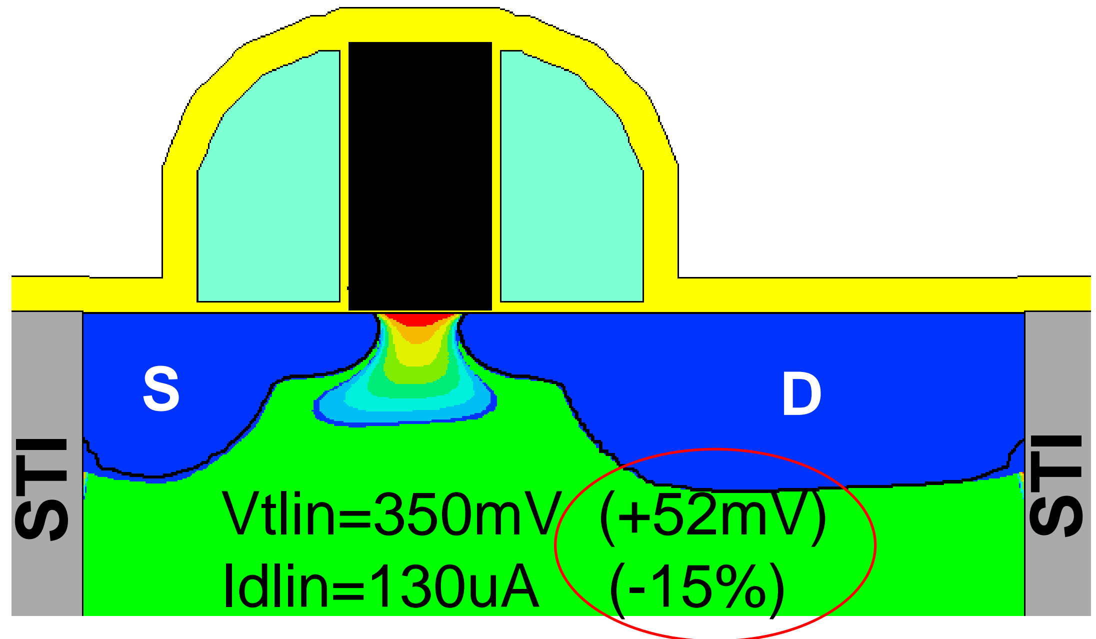
Threshold Variation Due to STI Proximity

Nested nMOSFET



Isolated nMOSFET



Maximum TED similar to the test nMOS with huge S/D area

Less TED with B asymmetry due to the different proximity of STI behind S & D

TED: transient induced diffusion

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Victor Moroz and Ignacio Martin-Bragado, MRS 2006 Spring

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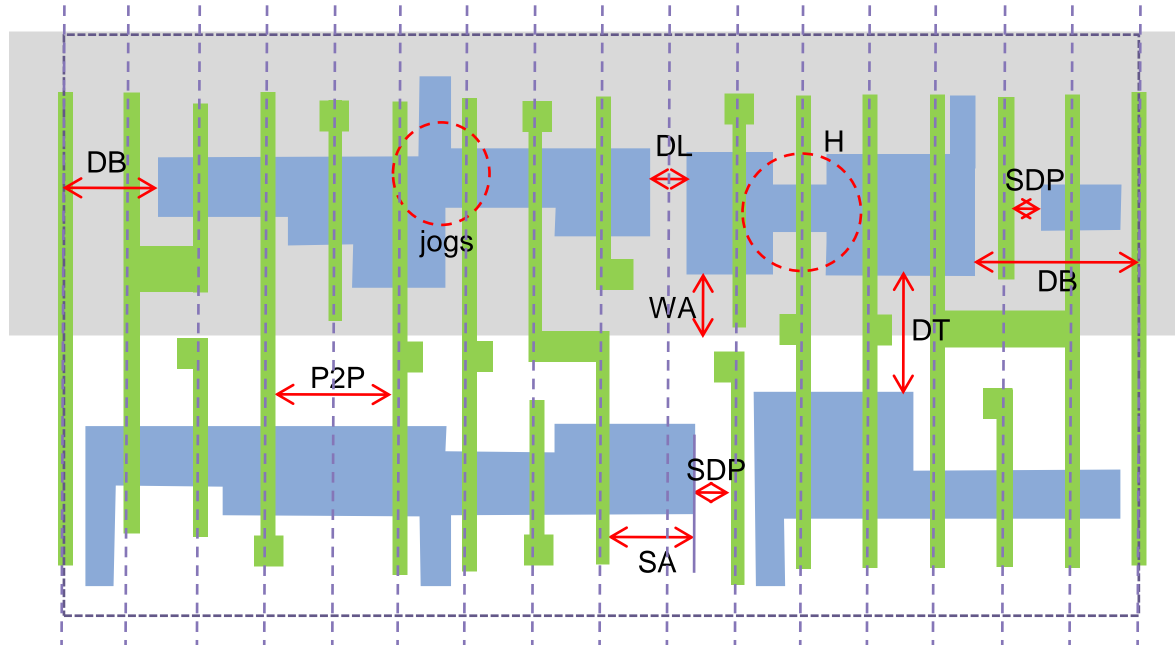
Complex Layout Effects



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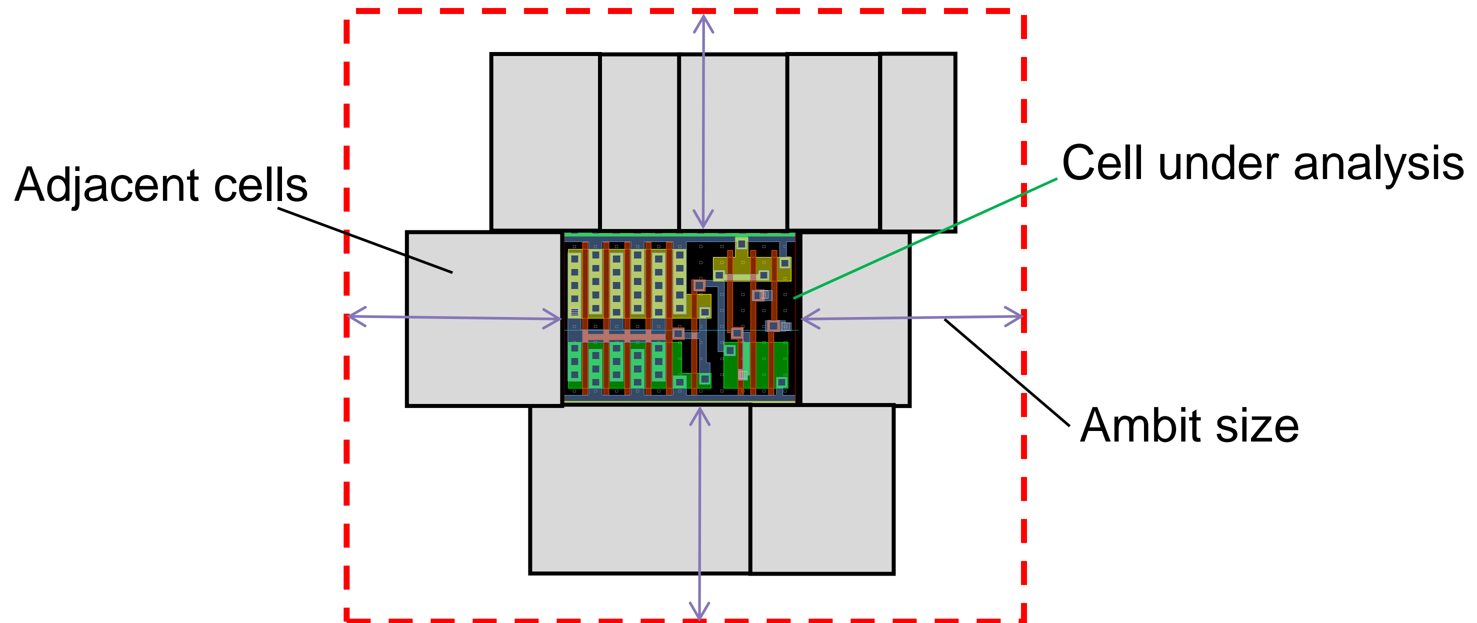
Typical Amount of Variations

Layout Variation	Typical I_{on} variation range	Typical V_{th} variation range
Length of diffusion (LOD) (SiGe or STI)	~30%	~50mV
Spacing to adjacent diffusion	~5%	~15mV
Active diffusion corners	~5%	~15mV
Poly spacing	~15%	~30mV
Poly corner rounding	~5%	~20mV
Well boundary (WPE)/ Dual stress liner (DSL)	~15%	~90mV
Contact to gate distance	~3%	~10mV

Cell Context as a Variable



Technology	0.18µm	0.13µm	90nm	65nm	45nm	32nm
Gate size (um^2)	5.3x2.0	3.7x1.4	2.6x1.0	1.8x0.7	1.3x0.5	0.91x0.35

- Ambit corresponds to the range of interaction
  - Ambit size = 1.5 um for litho and stress!
  - Gate size (2-input NAND) is smaller than the ambit size at 90nm and below.

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Variations: Causes and Effects

Effect	Physical Variation	Device Variation	Electrical Impacts	Core BSIM Parameters
Lithographic Proximity	Shape of poly gate, diffusion region	L, W	Ion, Ioff	L, LINT, DLC, W, WINT, DWC
Mechanical Stress	Mechanical strain, defect diffusion	Mobility	Ion	U0, VSAT, VTH0, K2, ETA0
Well Proximity	Channel doping	V_{th}	Ion, Ioff	VTH0, K2, U0
Implant Damage	Point defects (TED)	V_{th}	Ion, Ioff	VTH0, K2

Physical -> Electrical Variations

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Modeling Approaches

- Empirical Approach
  - As good as the test structures
  - Critical effects might be overlooked, without knowing where to look for
- Physics-based
  - Better predictability, despite unknowns
  - Decoupling of effects
  - More efficient usage of test patterns

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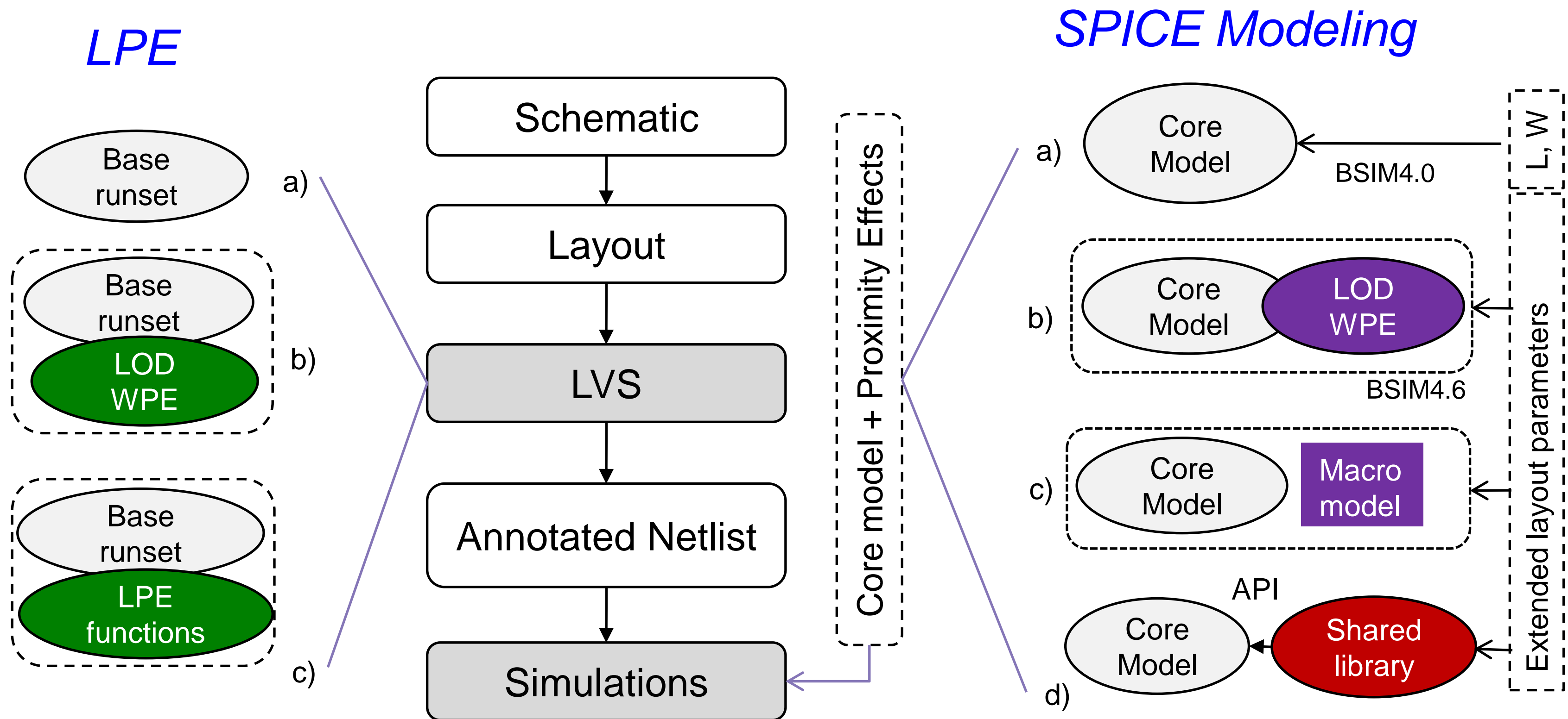
Adapting to Complex Proximity Effects



- Increasingly complex proximity effects lead to:
  - More development effects in LPE and modeling
  - Increased runtime during LVS and SPICE simulations

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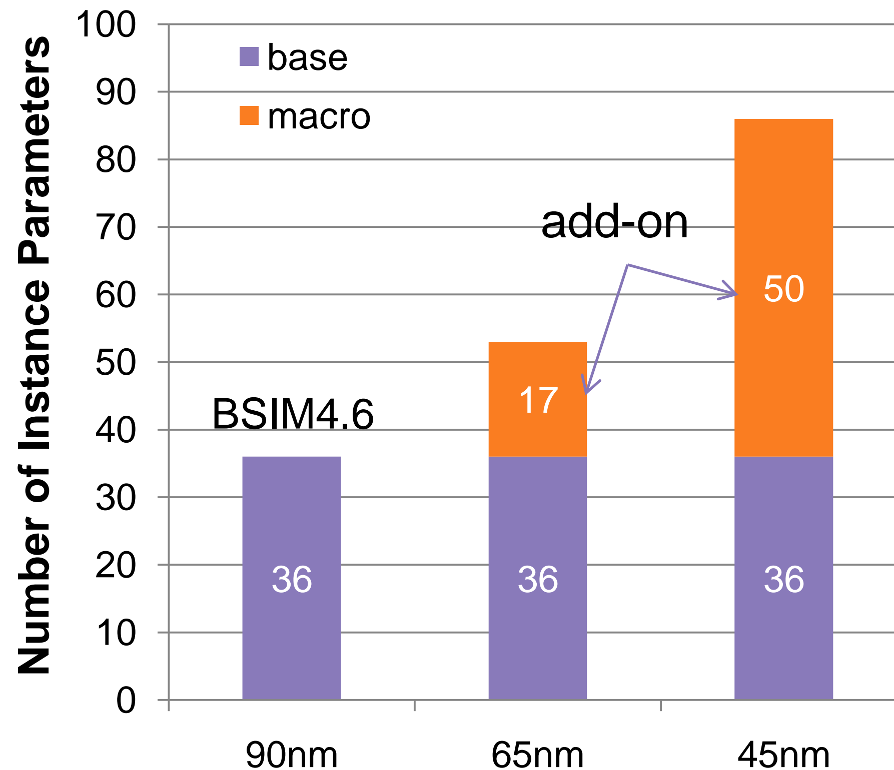
Increase in Number of Instance Parameters



- The number of LPE instance parameters are on the rise, due to the complexity of DFM effects.

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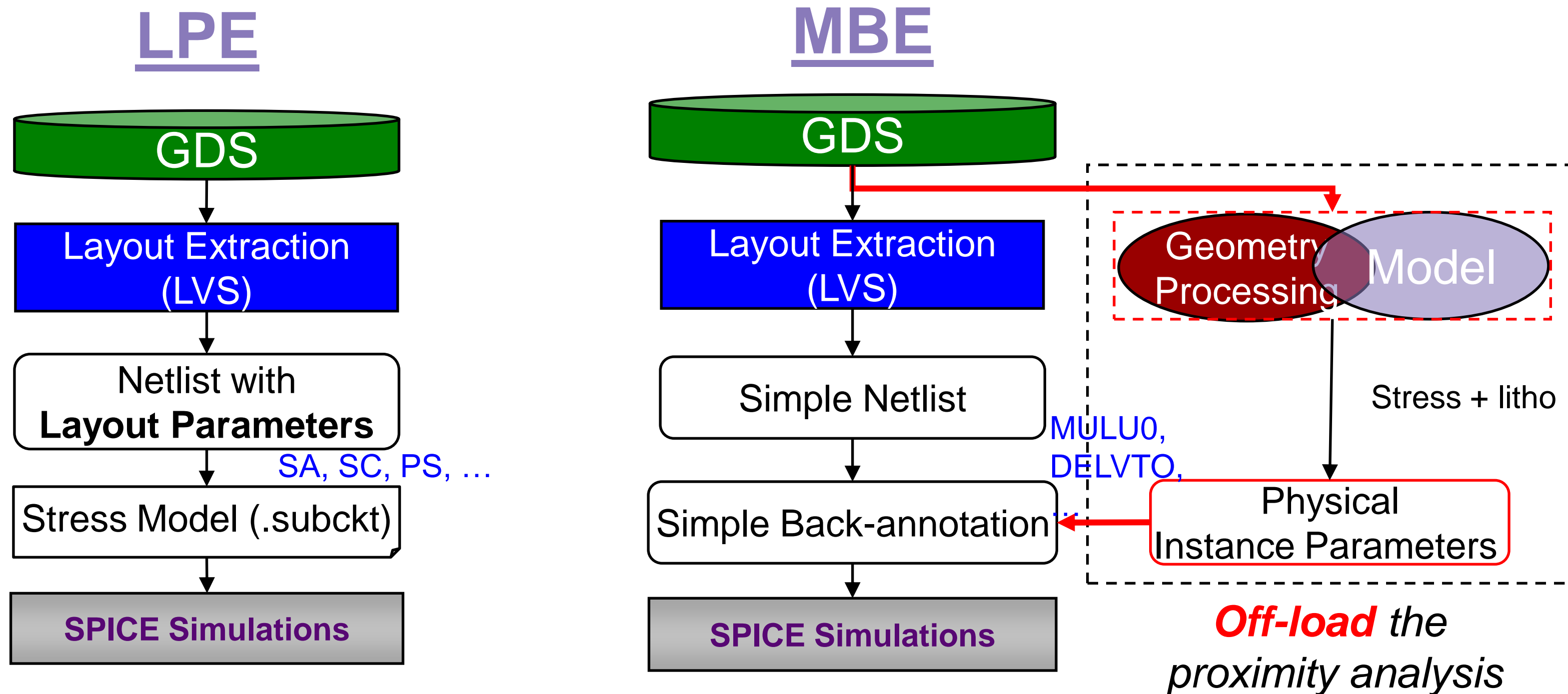
LPE v. MBE



- **Layout Parameter Extraction (LPE)**
  - Empirical and unscalable for complex proximity effects (Stress and Litho)
- **Model-Based Extraction (MBE)**
  - More physical, accurate, and predictable for complex layouts.

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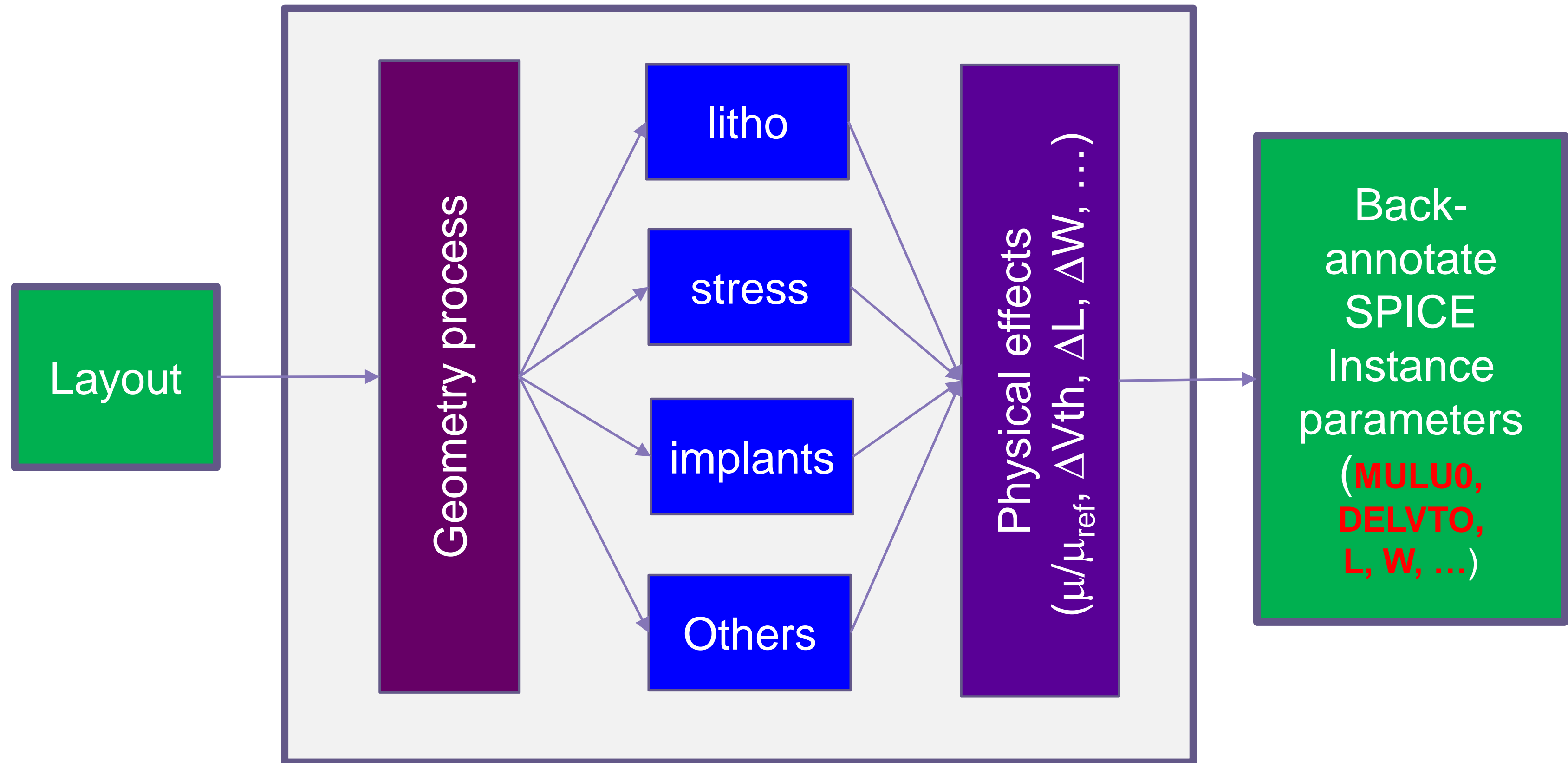
From Layout to SPICE Instance Parameters



- Integrate physical models with geometry processing.

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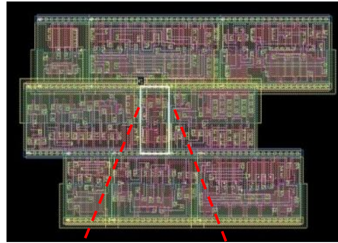
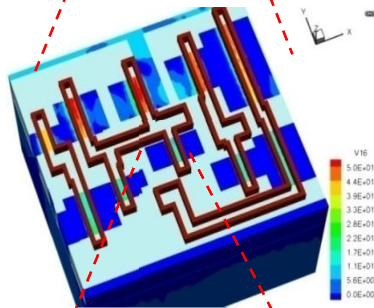
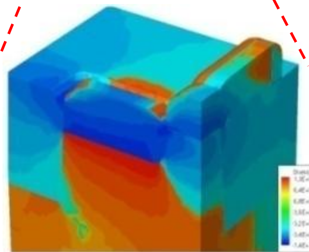
Strain Engineering and Modeling

Scale		Solutions	Applications
	Cell Level	MBE (Physics-based Compact Model)	• Cell optimization • Context sensitivity • Design exploration
	Multi-Device Level	TCAD (2D/3D FEA)	• Layout dependency • Process variability control • Forward looking design rules
	Device Level	TCAD (2D/3D FEA)	• Process optimization • Device characterization • Virtual prototyping

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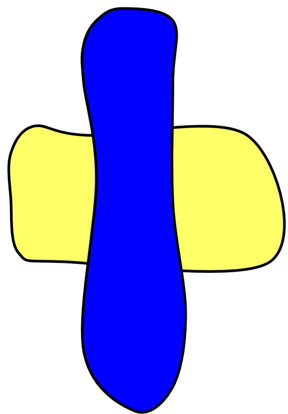
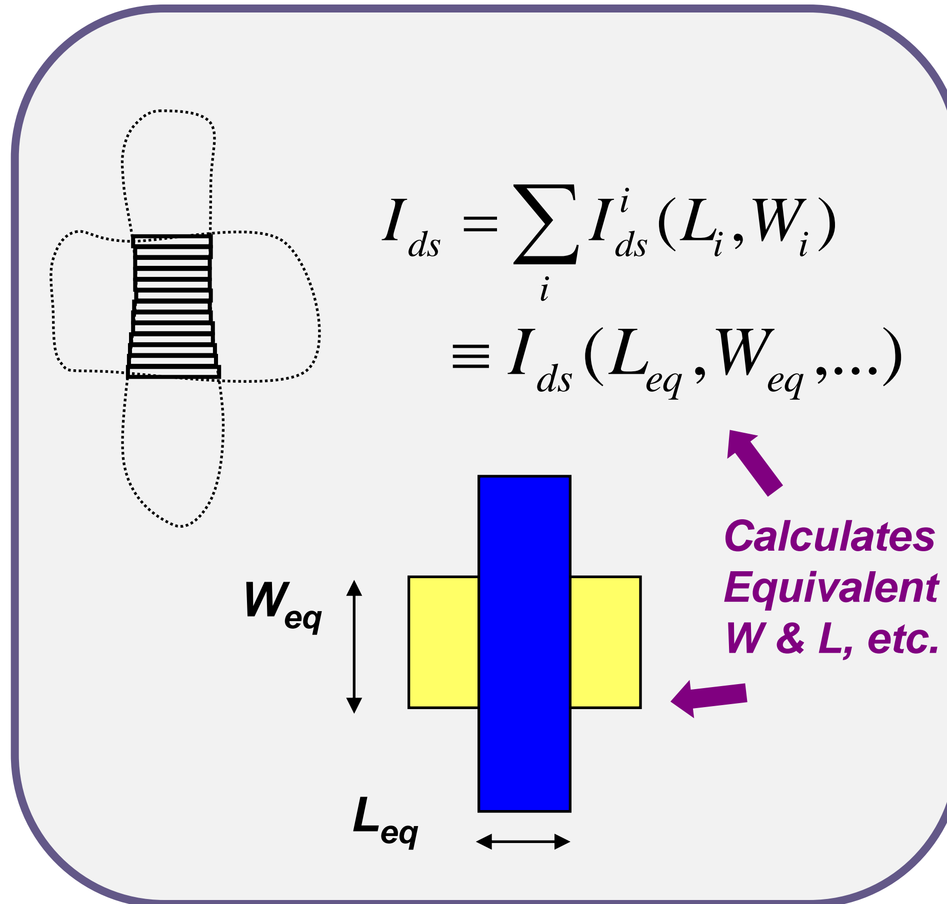
Contour to Electrical Analysis



Litho Contour (from Litho Simulator)



Annotated Spice Netlist

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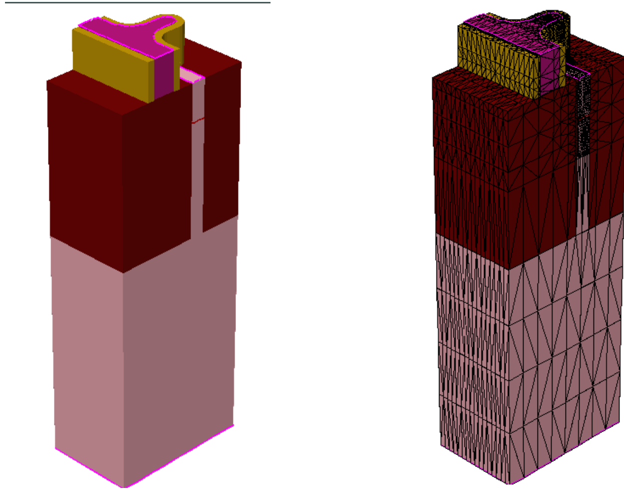
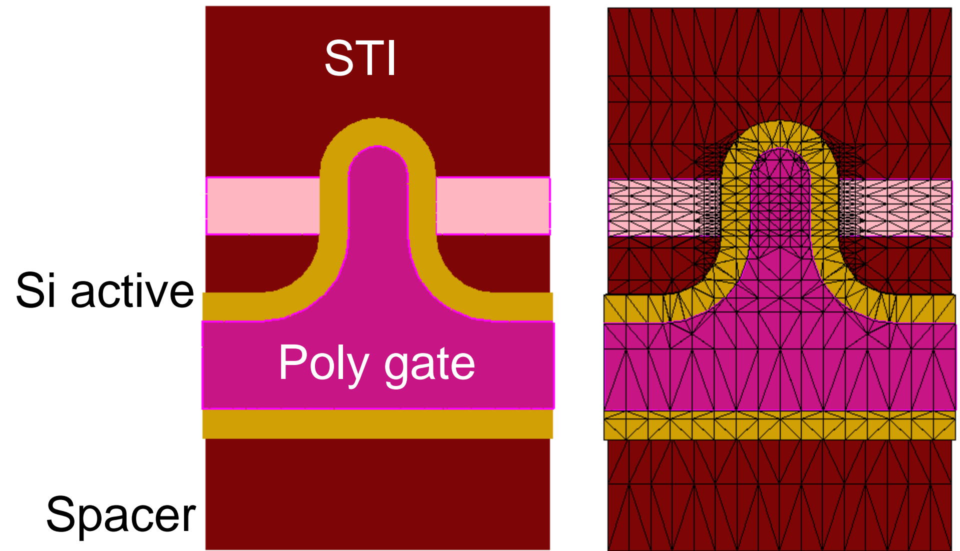
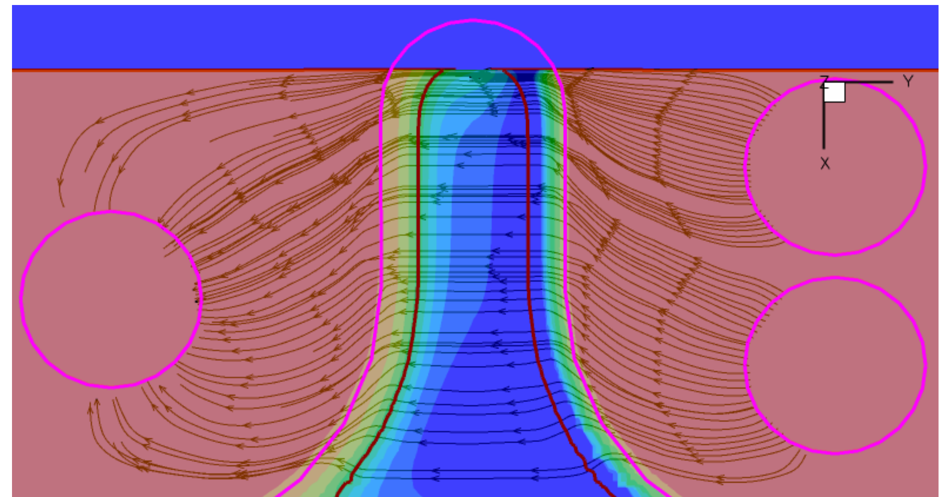
Gate Contour Simulations







• Current flows in parallel to channel length

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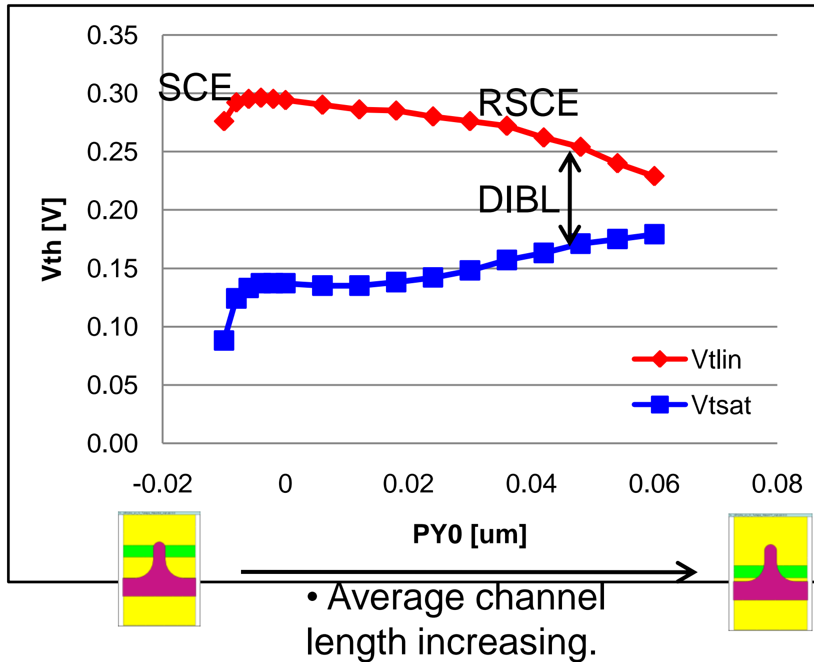
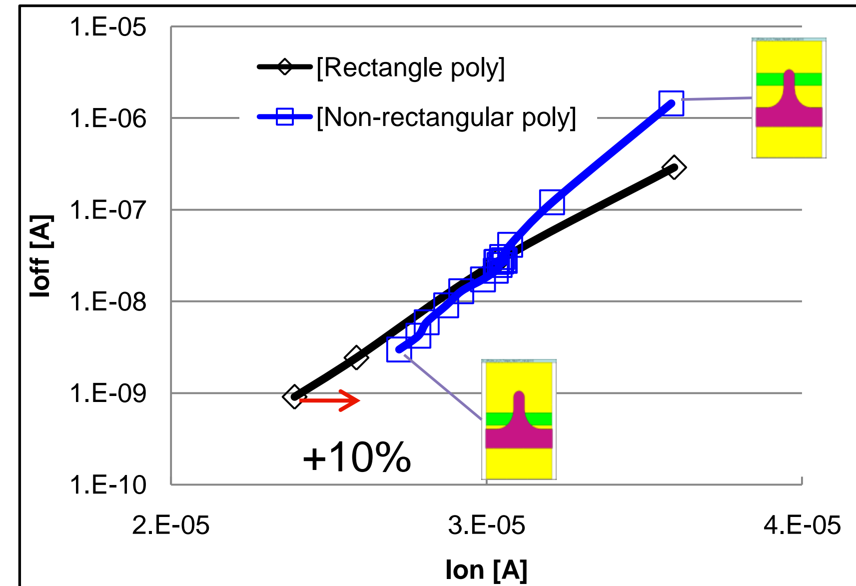
Non-Rectangular Poly Gate Shape

➢ **Threshold voltage**



➢ **I_{on}/I_{off} performance**



M. Choi et al. SPIE 09

- Poly flare-out is beneficial
- 10% I_{on} gain at a fixed I_{off} or 3x reduction in I_{off}

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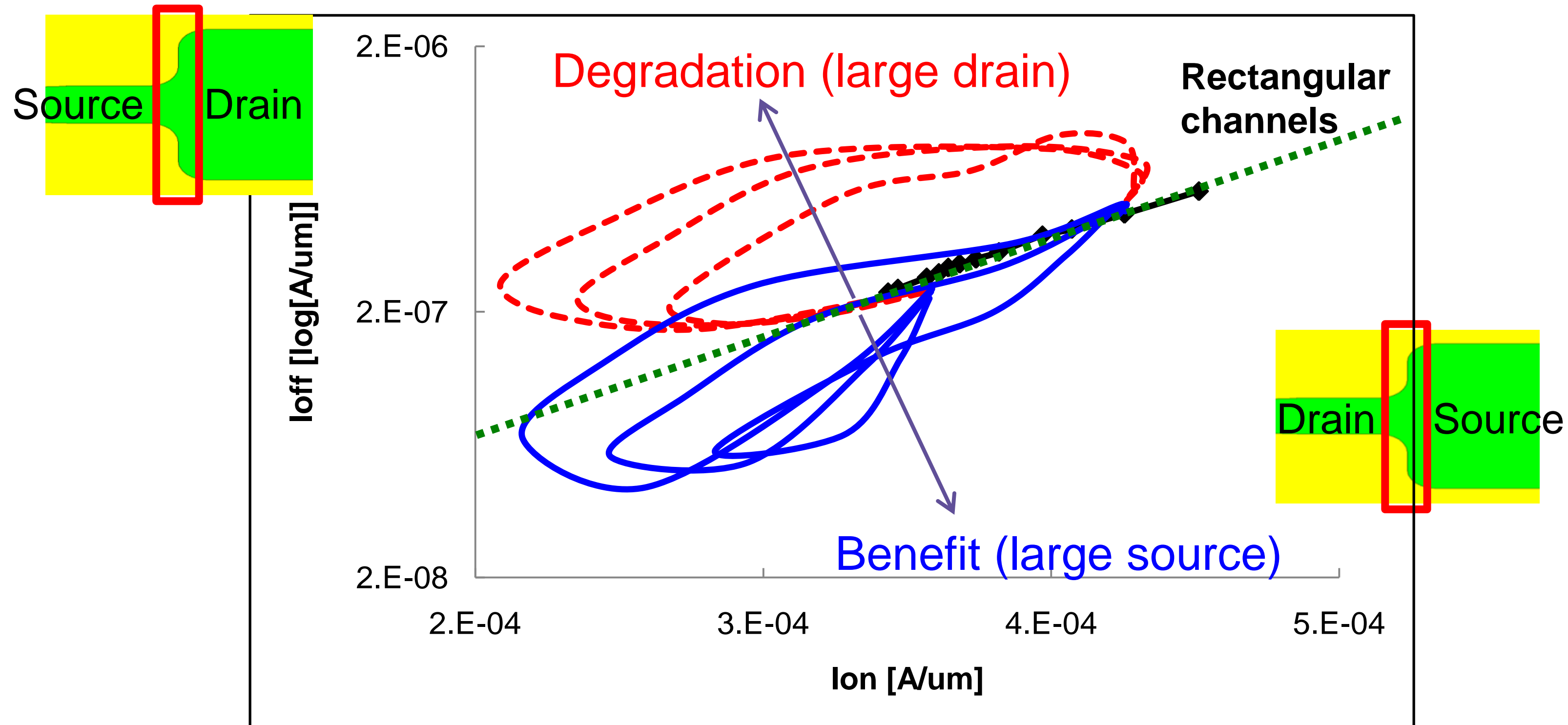
Active Rounding : I_{on}/I_{off} Performance



- Large source structure provides better performance
  - 10% Ion gain or 3x Ioff reduction
- Large drain structure degrades performance
  - 50% Ion degradation or 3x Ioff leakage

M. Choi et al. SPIE 09

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Outline

- Introduction
- Modeling Considerations
- Tackling Variability
  - Accurate modeling
  - Understanding sensitivity
  - Prevention
  - Optimization
  - Visibility to designers
  - Margin
  - Efficient design flow
- Summary

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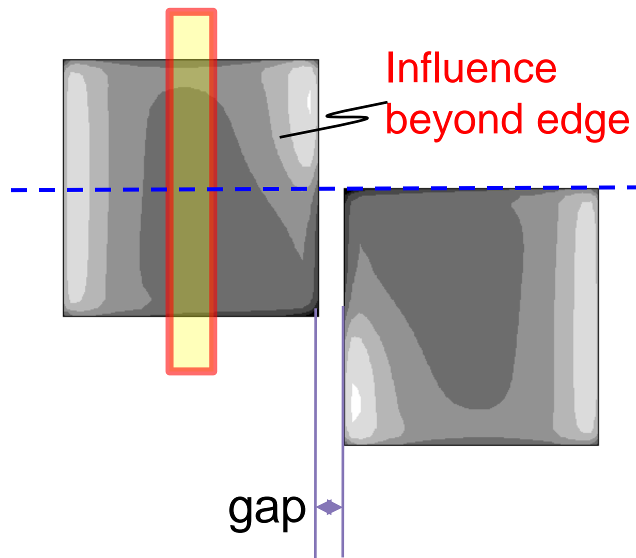
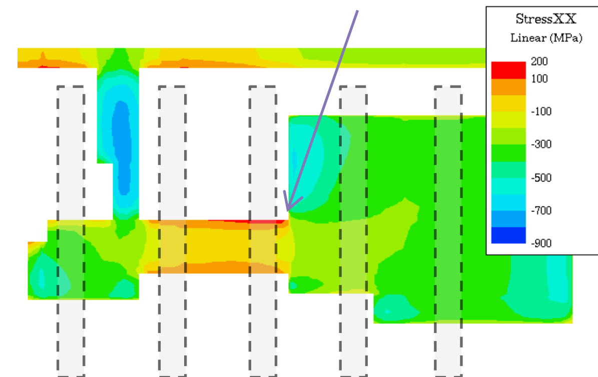
Stress Field





- Stress is a field that penetrates across isolation and beyond edges.

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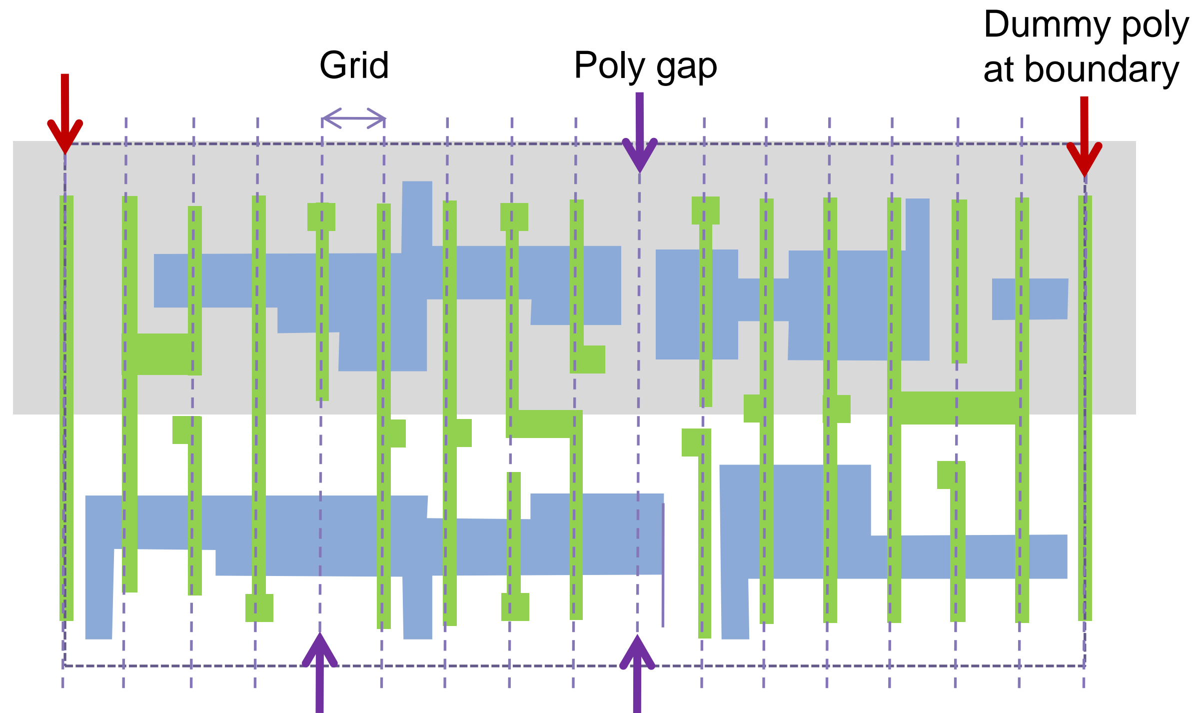
Prevention



- Regularity and restrictive design rules (RDR) are necessary to mitigate the primary variability.
- But RDR is not sufficient, as the need for layout flexibility will persist, due to density and performance constraints
  - Poly spacing variation still exists, despite effort to comply with RDR – poly-on-grid
  - Active diffusion jogs and corner rounding remain pervasive.

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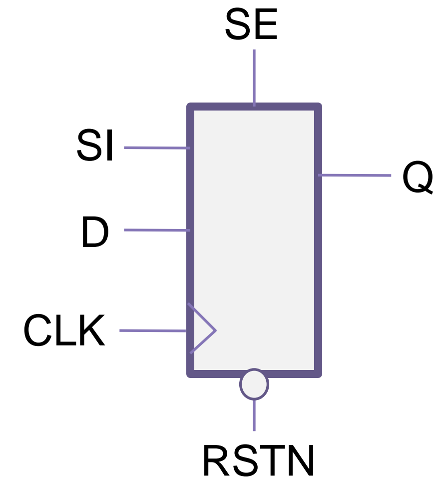
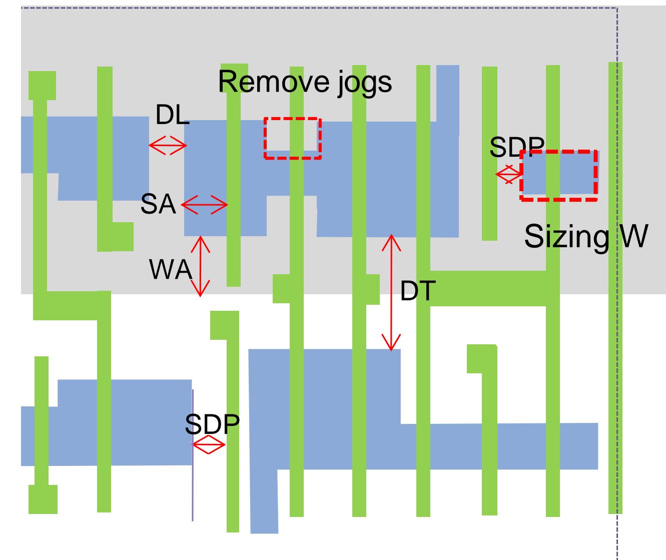
Optimization

- Objectives
  - Minimize sensitivity
  - Match Idsat
  - Delay/Leakage
- Focus on critical devices
  - Ignore non-critical ones (enable, reset, …)
- Adjustments
  - Sizing W, remove jogs, adjust distance to n-well, …
  - Cell placement with desirable neighbors





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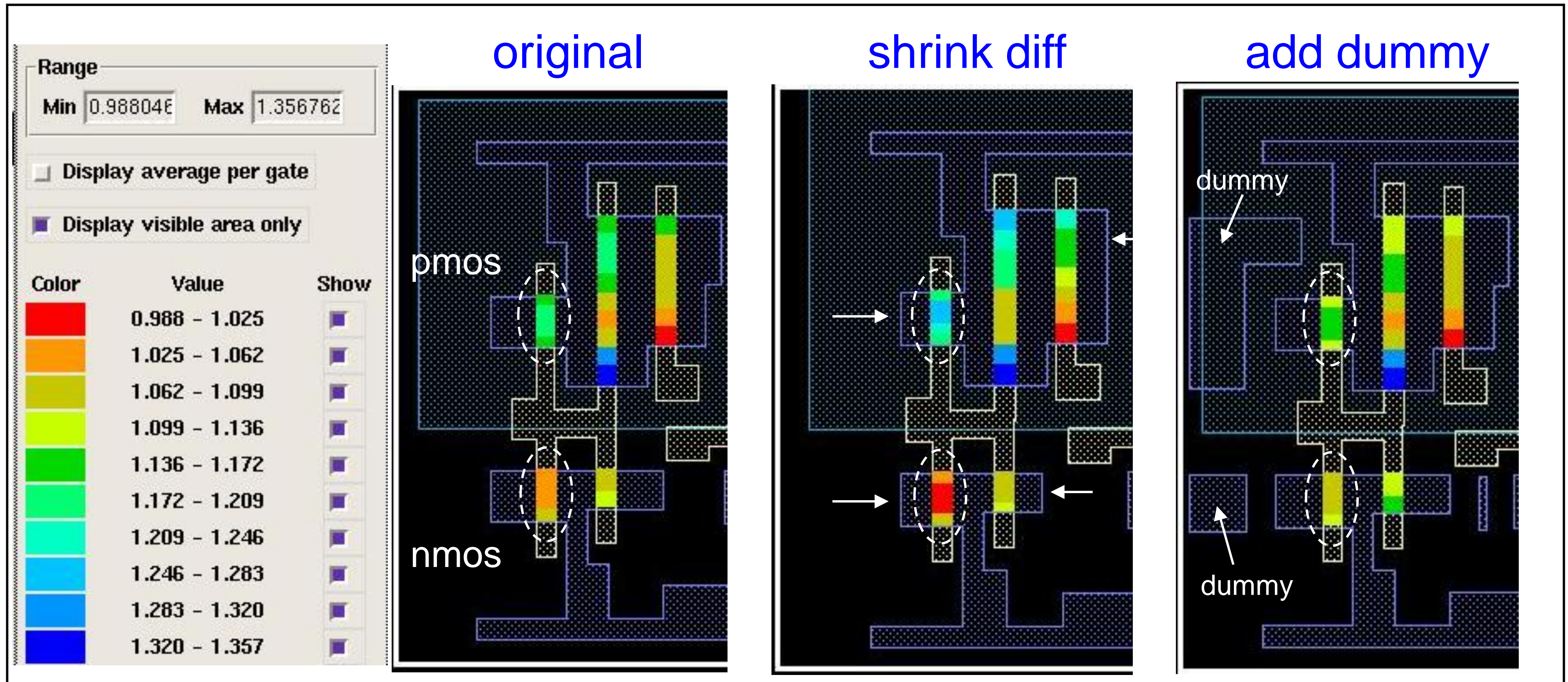
What-if Analysis



- weaken nmos
- enhance pmos

- enhance nmos
- weaken pmos

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Losing Visibility …

LPE annotated netlist …

```
M1 N_2 N_93 N_9 N_135 pm  l=0.032000u w=0.40000u ad=0.048262p pd=1.054000u as=0.028630p ps=0.549000u
nrd=0.534977 nrs=0.233352 ka=0.284000u kb=0.118000u ka1=0.284000u kb1=0.118000u ka2=0.284000u kb2=0.118000u
+                 ka3=0.284000u kb3=0.118000u sca=15.009148 scb=0.014816 scc=0.001477 xp=0.244435u
+                 xp1=0.230865u xp2=0.174918u xp3=0.191948u xa=0.206750u ka4=0.166915u xb=0.179857u
+                 xb1=0.181837u fx=3.862724u fx1=3.855471u fy=0.338502u fy1=0.251403u fy2=0.324598u
+                 rs=5.430328u rw=0.634072u *xy(4.047 0.1445)

M2 N_2 N_92 N_9 N_135 pm l=0.032000u w=0.40000u ad=0.042536p pd=1.026000u as=0.028630p ps=0.549000u
nrd=0.533926 nrs=0.233352 ka=0.104000u kb=0.298000u ka1=0.104000u kb1=0.298000u ka2=0.104000u kb2=0.298000u
+                 ka3=0.104000u kb3=0.298000u sca=14.969629 scb=0.014816 scc=0.001477 xp=0.140000u
+                 xp1=0.140000u xp2=0.140000u xp3=0.140000u xa=0.145771u ka4=0.154446u xb=0.178830u
+                 xb1=0.180733u fx=4.010791u fx1=4.004751u fy=0.338502u fy1=0.251403u fy2=0.324598u
+                 rs=5.510477u rw=0.634072u *xy(3.867 0.1445)
```

- Designers' questions:
  - What's the actual driving strength of transistor M1 ?
  - How is M1 different from M2, both having the same W & L?

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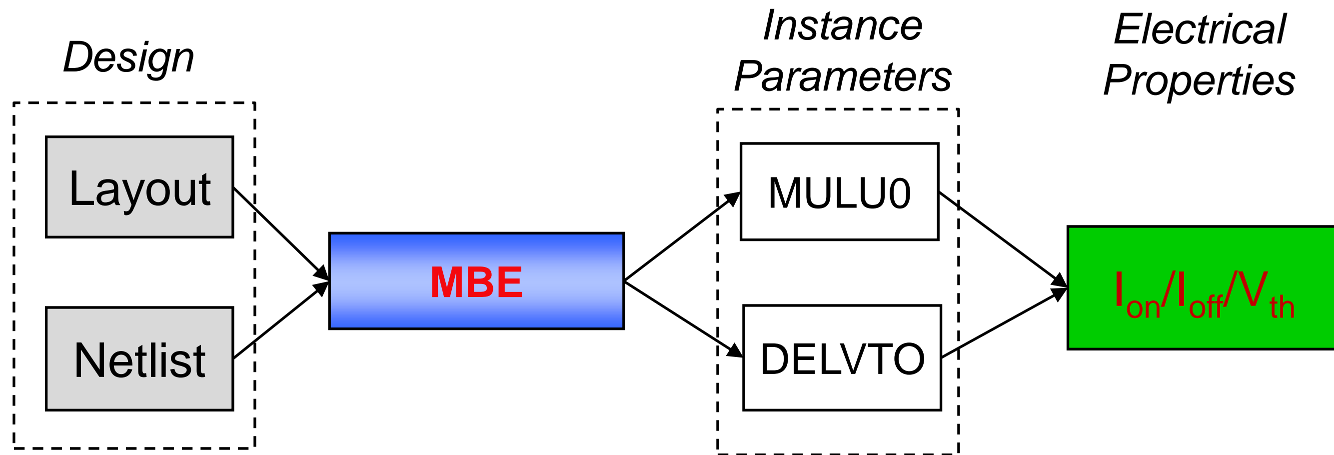
From Layout to Electrical …



MI47 VSS CDN:F67 XI180-NET6:F68 VDD pm l=0.032u w=0.4u ad=0.034174p nrd=0.37971 nrs=0.266667
\+ pd=0.678261u ps=0.46u as=0.024p
\+ MULU0=1.054 DELVTO=-0.022 **$Ion=0.0002595 $Ioff=1.325e-08 $Vtsat=0.069489**

- Directly relate layout to electrical properties (I_{on}, I_{off}, V_{th}) for each transistor in design

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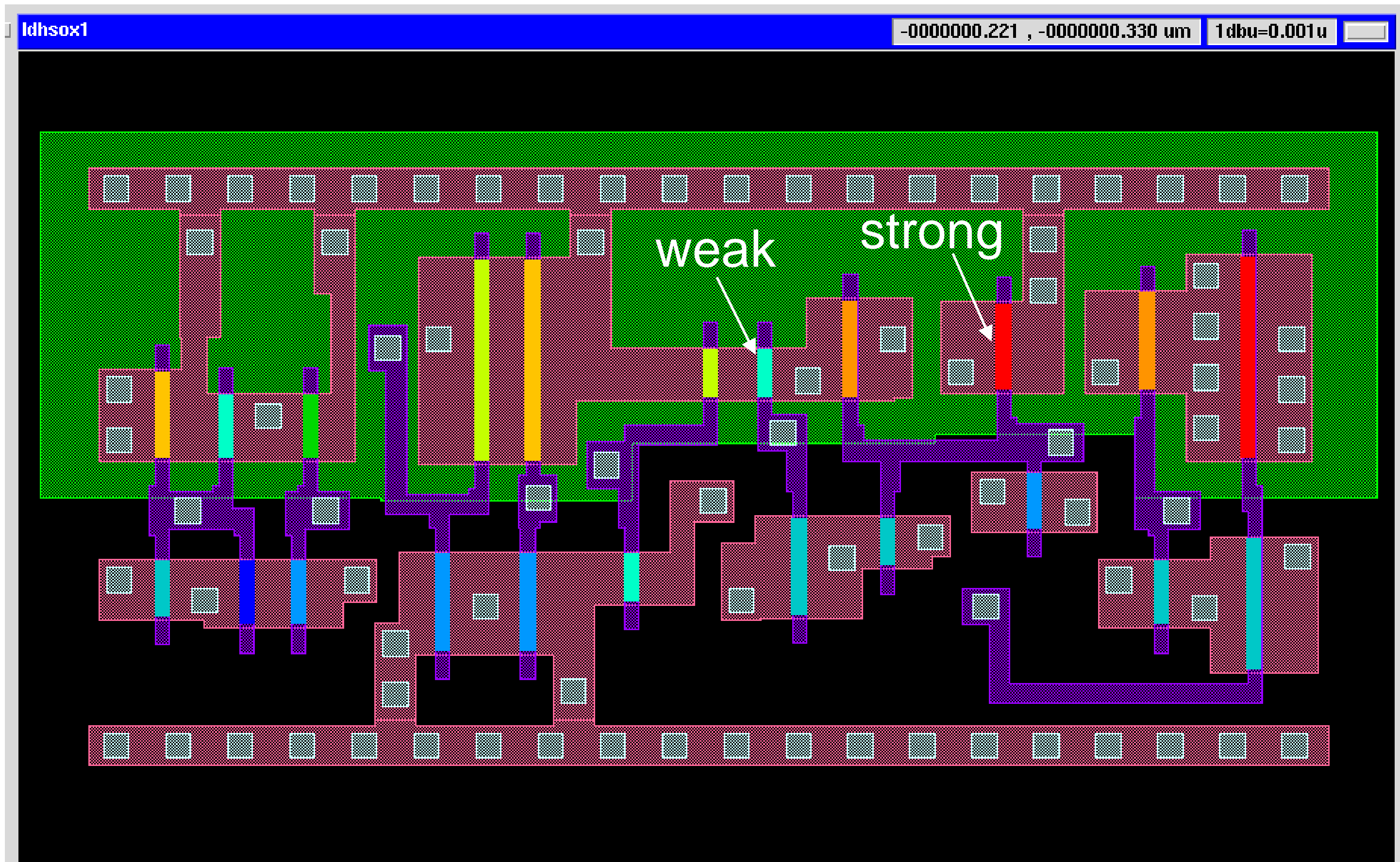
Visualization : Electrical Variation Across a Cell



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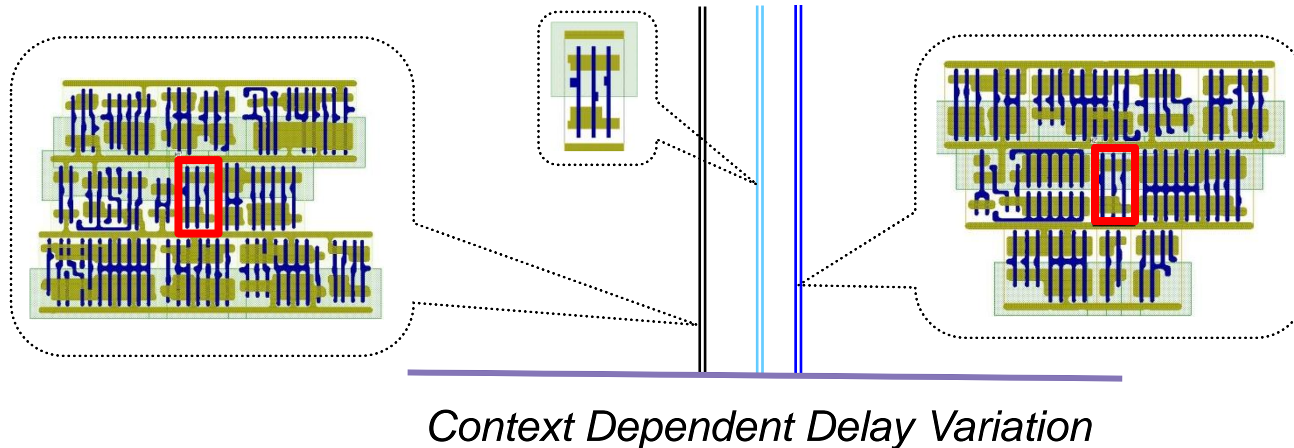
Analyzing Cell Context Effects



Context Dependent Delay Variation

- Context dependent timing variation can be evaluated to determine
  - Sensitivity
  - Distribution
  - Derating factor, …

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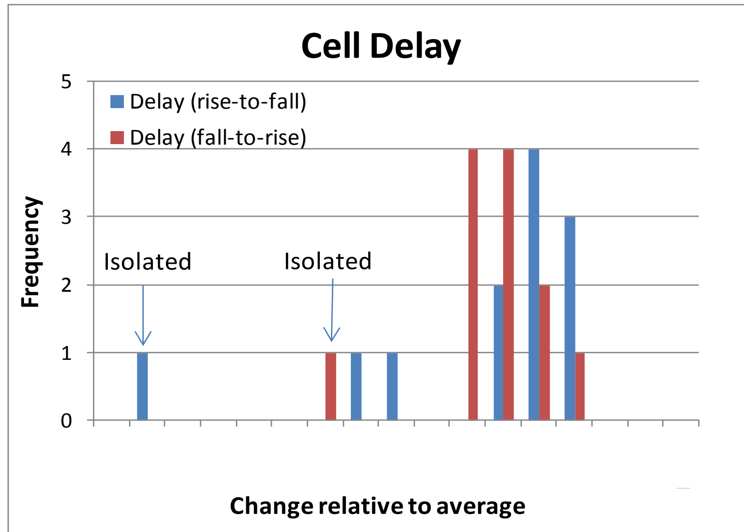
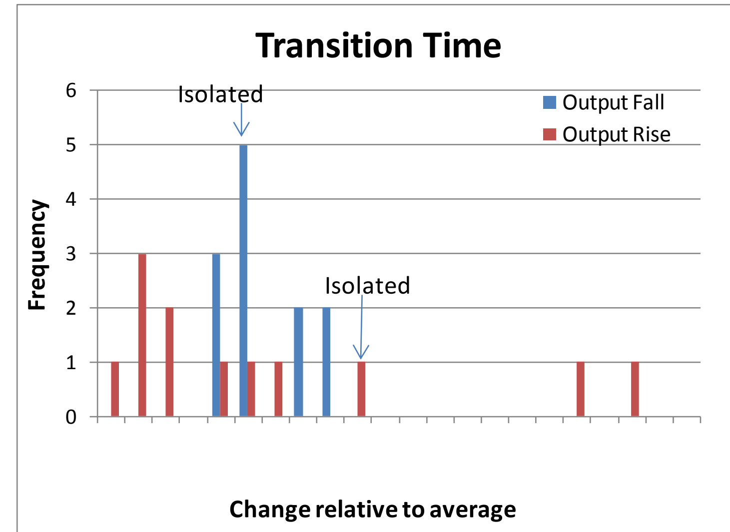
Example: Context Dependent Timing Variation





- Context analysis reveals timing variations (delay/transition), and best and worst case neighbors.

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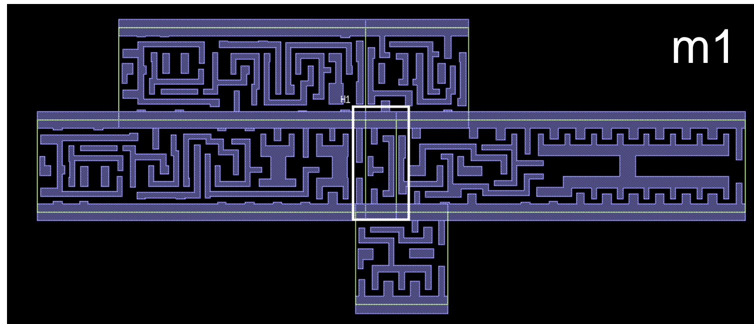
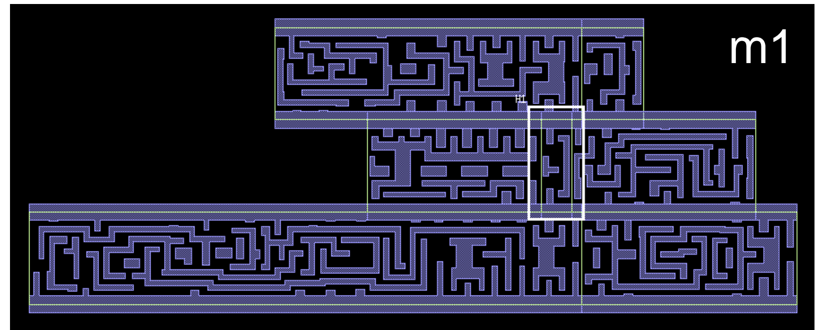
Interconnect Context



Case 1



Case 2

- Capacitance is dependent on cell context, due to coupling and metal density variations.

Net	N1	N2
diff	136.70%	47.45%

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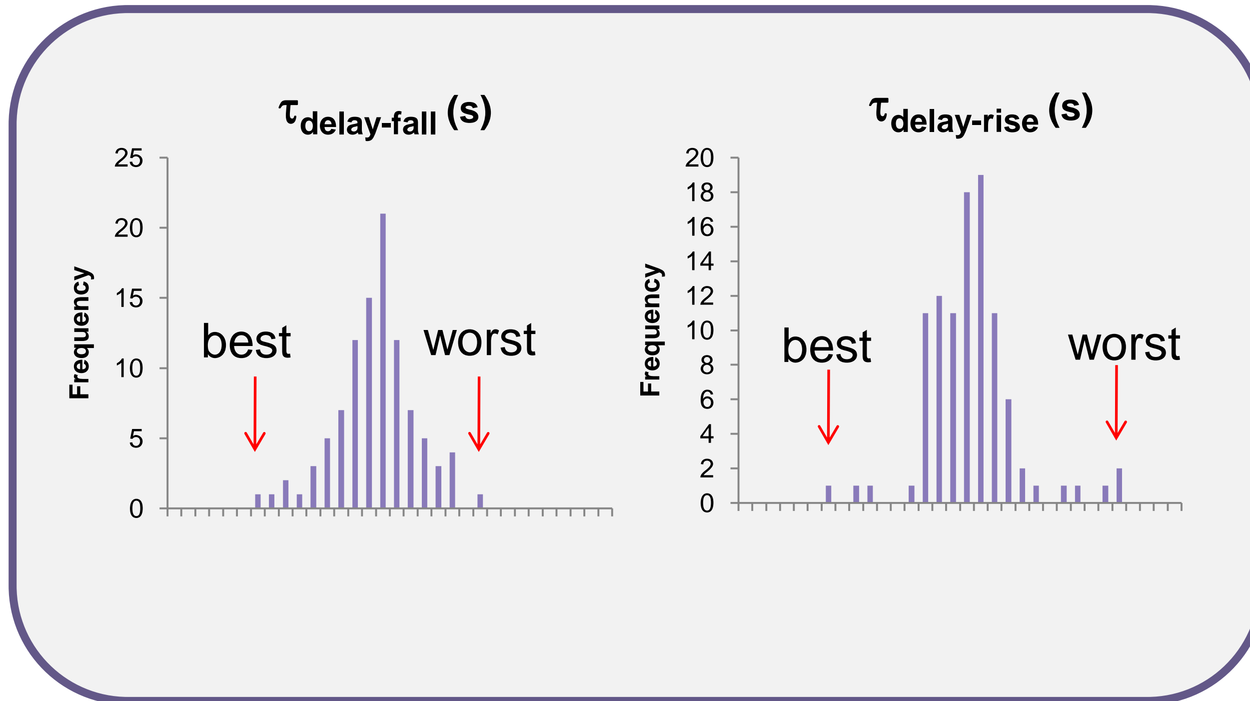
Context Distribution



- Context analysis reveals timing variations, and best and worst case neighbors.

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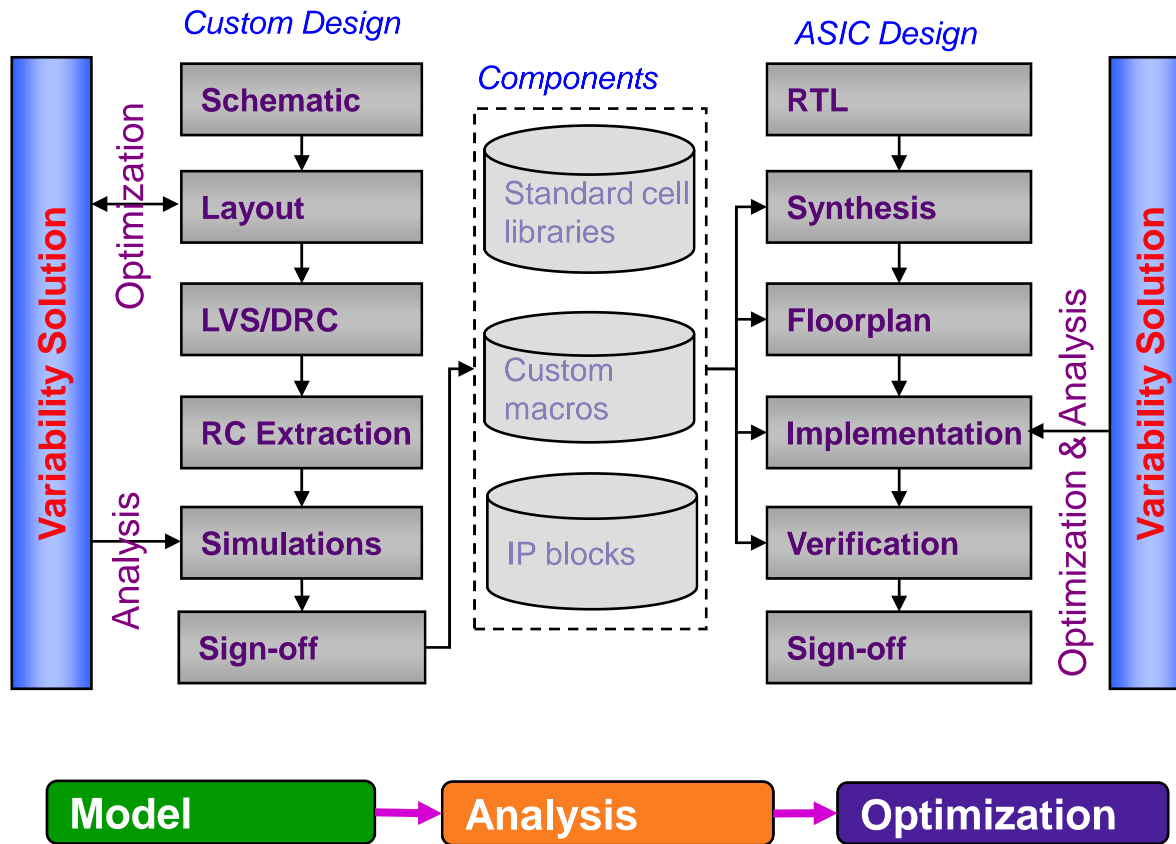
Global View

- Beyond circuit simulations …



Model → Analysis → Optimization

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Open Questions

- Is it possible to standardize the proximity models?
- How to quantify the trade-offs between RDR and design flexibility in actual chips?
- How to take advantage of variability for performance and cost trade-offs?
- How to quickly estimate circuit sensitivity to individual components and their interactions?
- How to perform concurrent optimization to close the design gap between pre and post layout in custom circuits?
- Anything new in FinFET strain engineering?
- …

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Summary

- Layout proximity effects arise from interactions between design and process
- The stress variability in design surpasses litho at 45nm and below
- Understanding of the underlying physics is essential to develop practical solutions to tackle the electrical variability
- Design methodology and efficiency are important as well

THANK YOU

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