Modeling the Dishing and Erosion in Copper CMP

SFR Workshop
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Berkeley, CA

2001 GOAL: Develop periodic grating metrology to support integrated CMP model (with Dornfeld and Talbot) (done); Define research plan to explore the non-uniformity issues in the copper damascene process

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Motivation

- Non-uniformity problems on patterned wafers during copper CMP become the bottleneck in improving fabrication yield.
- First-principle based model can help optimize the operation of CMP and drive the technology further in the long run.
- The decoupling of systematic interconnect variation (due to CMP) from the total variability can help IC designers try more aggressive circuit design.*.

* References:
[1] Y. Liu; S.R. Nassif et. All, “Impact of interconnect variations on the clock skew of a gigahertz microprocessor,” Proceedings of the Design Automation Conference, 2000. pages 168 –171
[2] Z. Lin, C.J. Spanos et. All, “Circuit Sensitivity to Interconnect Variation," IEEE Trans. Semiconductor Manufacturing, Vol. 11, No.4, November 1998.

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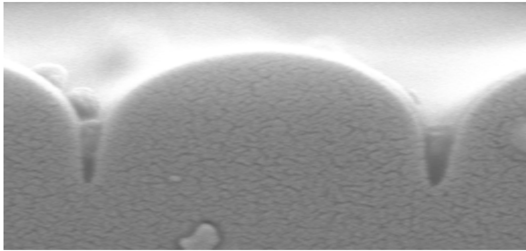
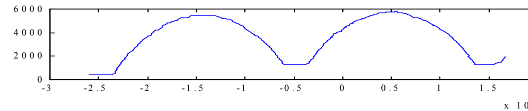
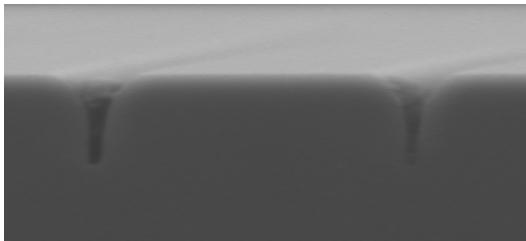
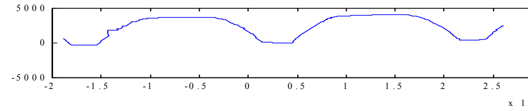
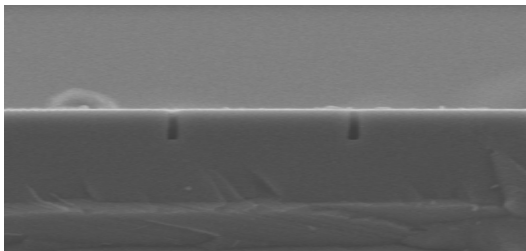
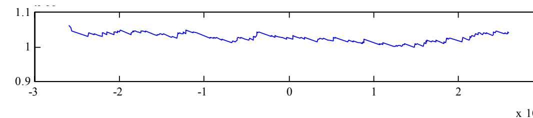
Previous Experiments on Oxide CMP

SEM AFM Scatterometry

- Extracted profiles match SEM pictures with 5nm precision
- Scatterometry is the non-destructive, faster metrology for CMP

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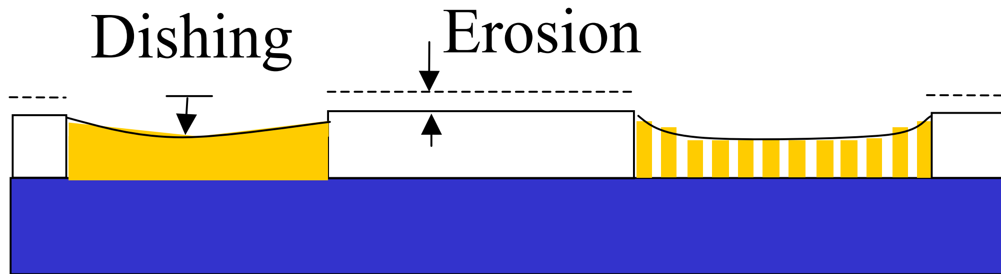
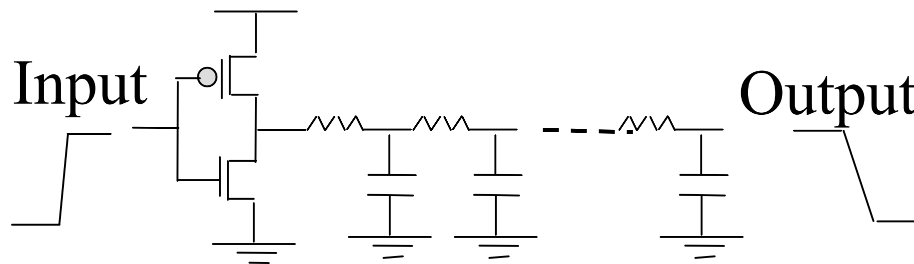
From Oxide to Copper

- Transferring ideas from the oxide CMP modeling efforts
  - Idea of the planarization length and window
  - Idea of the Berkeley 2000.4 mask design
- Transferring results
  - The metrological capability of library-based scatterometry which gives non-destructive measurements on oxide profiles
  - The proportionality between the effective pattern density and the polishing rate
  - The step height dependency analysis
- Build new models on oxide erosion and copper dishing

Dishing and Erosion Effects





- Oxide erosion and Cu dishing in the Cu damascene process are the limiting factors for yield improvement.
- A simple HSPICE simulation shows that 100Å (~5%) Cu loss may degrade the interconnect performance by ~4.6% for the 0.25μm technology.

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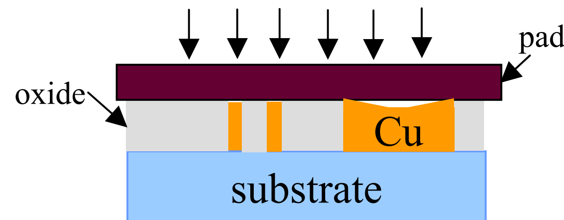
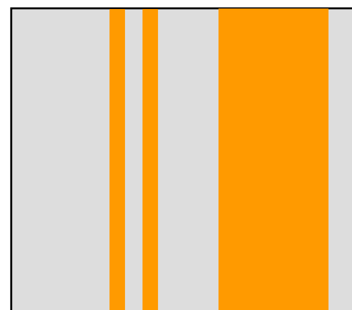
Framework on Erosion Modeling

- Erosion can be treated as a oxide polishing problem. We need to use the “integrated” effective pattern density, which considers the ratio of the copper area within the window

Cross-sectional view



Top view



Copper lines are in partial contact with the pad, so the effective pattern density will be based on the area of copper in the window (with planarization length)

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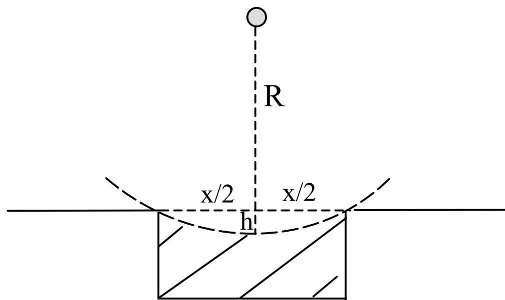
Frame Work on Dishing Modeling

R: average radius of the pad asperity ~30μm



R: average size of the pad asperity
H: dishing height
X: the copper line width

$$\frac{R}{\sqrt{\left(\frac{x}{2}\right)^2 + h^2}} = \frac{\sqrt{\left(\frac{x}{2}\right)^2 + h^2}}{h}$$

Solve for h we get $$h = \frac{R - \sqrt{R^2 - x^2}}{2}$$

When x<<R $$h = \frac{x^2}{4R}$$

For x=1μm, R=30μm, h is About 8.3nm

- Dishing is strongly related to pad asperity, Young's modulus of the pad and the chemical aspects of slurry.
- The primary calculation results based on this model show that the dishing percentage (conductivity loss ratio) is proportional to the square of line width.

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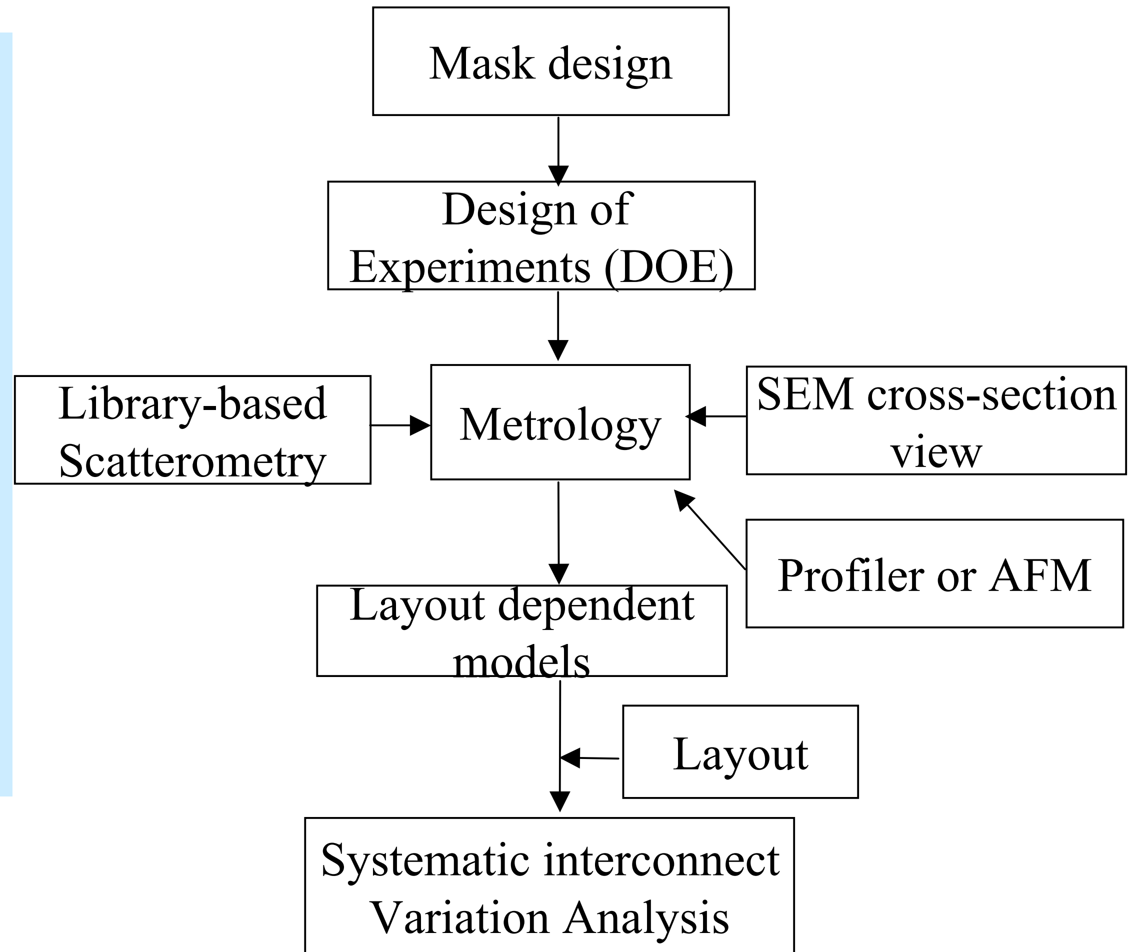
Experimental Plan

- Mask will include E-test structures with different pattern density, line width, pitch size, etc.
- Scatterometry gratings will also be included.



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2002 and 2003 Goals

- Finish mask design, design of experiments and copper damascene process data collection (with Dornfeld and Talbot), by 8/31/2002.
- Develop comprehensive chemical and mechanical model (with Dornfeld and Talbot); Evaluate the CMP variation impact on interconnect, by 8/31/2003.