DfM @ IBM: status, challenges, opportunities

'Integrated Modeling Process and Computation for Technology' Seminar

Lars Liebmann et al., IBM

Net

Industry is in dire need of design-technology co-optimization.

Current DfM proposals fundamentally can't work.

Industry is in no position to invent revolutionary DfM.

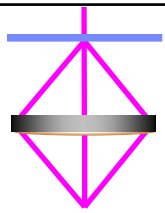
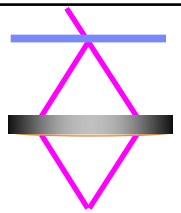
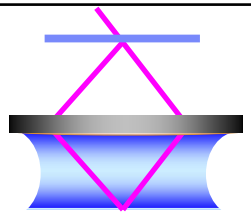
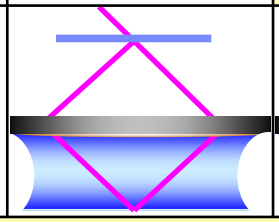
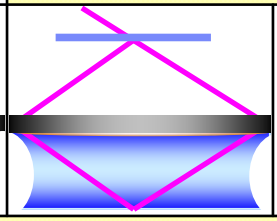
If we continue to try to milk established solutions we will fail.

Industry-Academia collaborations are in the best position to seed innovation.

Discuss these views, brainstorm on potential solutions, do the research.

Benefit: there may still be a Semiconductor industry to graduate into.

Scaling through 'Discontinuous Innovation'

Node, Year	90nm, '03	65nm, '05	45nm, '07	32nm, '09	22nm, '11	15nm, '13
Pitch	250nm	200nm	140nm	100nm	~70nm	~50nm
λ	193nm					
NA	.75	.85	1.2	1.35		
k_1	.5	.44	.44	.35	.25	
						=
Common Patterning Solutions	Optical Proximity Correction					
		off-axis illumination with assist features				
			water immersion			
				double patterning		
					Source-Mask Optimization	
						SIT
Common Process Solutions		strained silicon				
			air-gap metallization			
				high-k metal gate		
					innovative interconnect	
						fin-FET

Terminology: ‘DfM’ vs ‘MfD’

DfM (Design for *Manufacturability*):

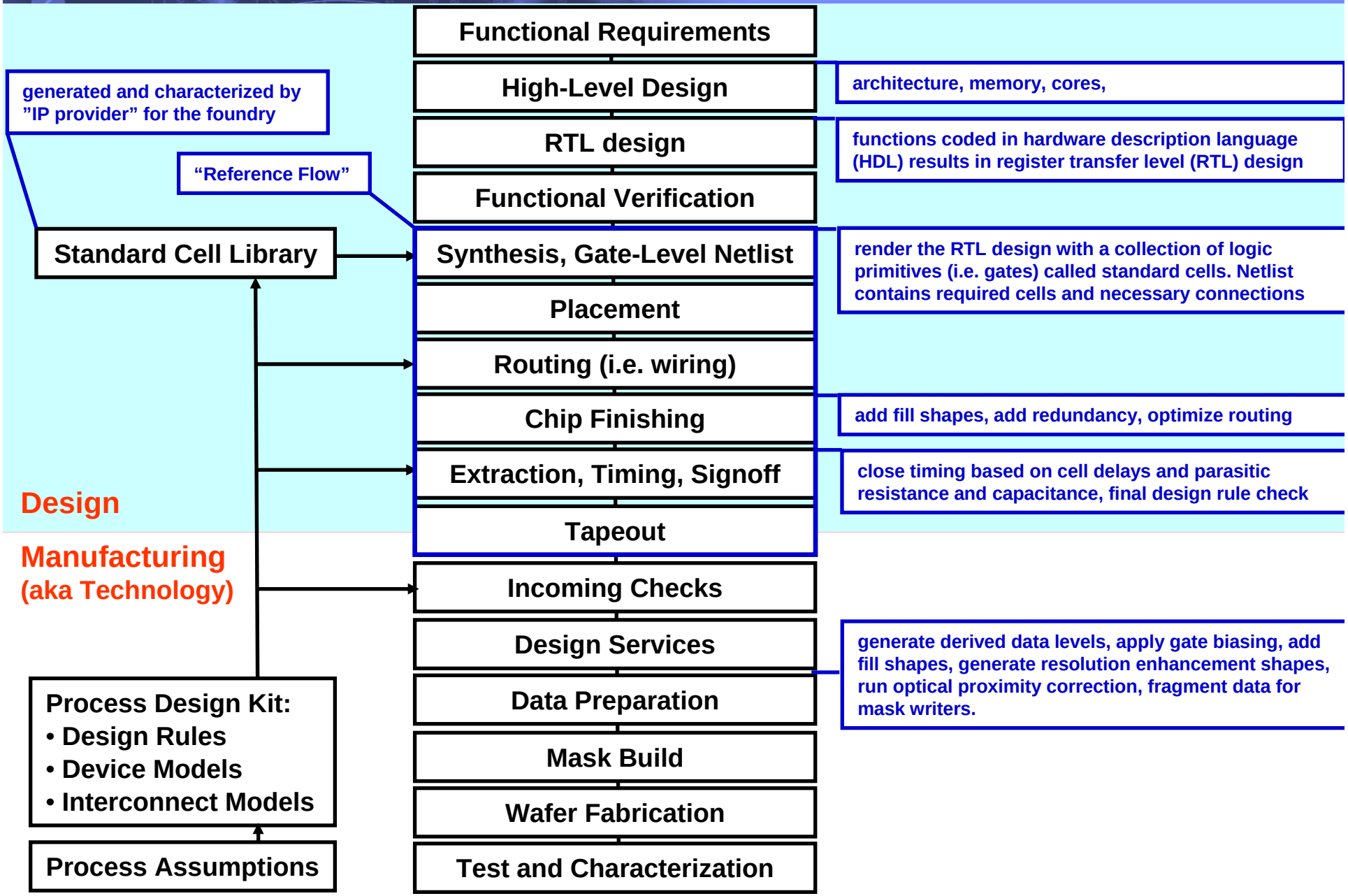
process-aware actions taken in design to improve power/performance/yield/area/time-to-market

vs

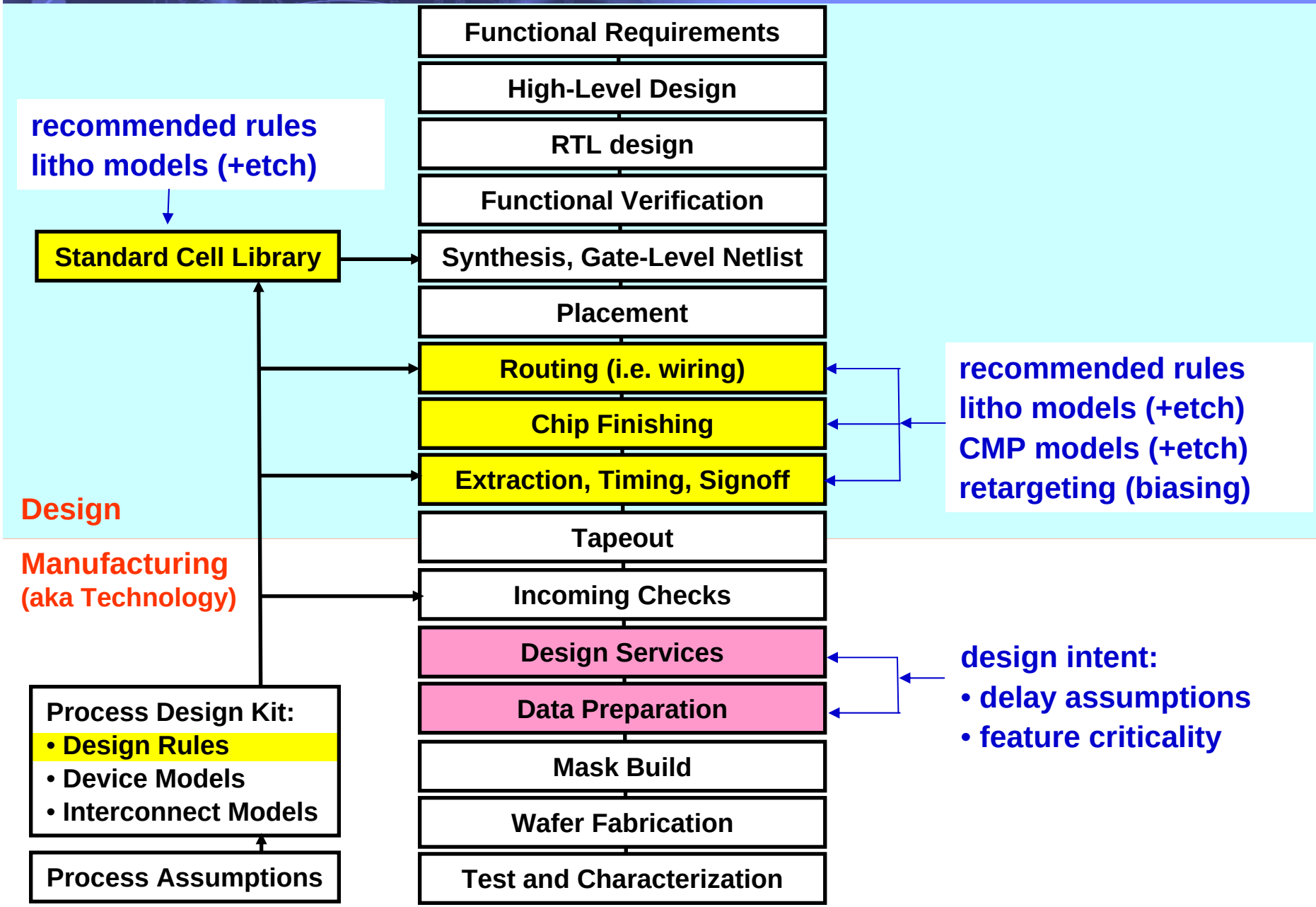
MfD (Manufacturing for *Designability*):

design-aware actions taken in manufacturing to improve power/performance/yield/area/time-to-market

Terminology: ‘Design’ vs ‘Manufacturing’

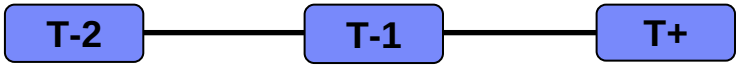


DfM vs MfD



Technology Node Timeline

TMR-3yrs	TMR-2yrs	TMR-1yr	TMR+1yr	TMR+2yrs	TMR+3yrs
design guidelines defined	design rules defined cell image and power grid decided	library design finalized design flow qualified	production tapeouts ramp volume		
technology elements defined	integrated process running			match chip yield of previous node	mature yield
extrapolated litho models	litho models calibrated to development tool	development litho + etch models first CMP models			



…..repeat on a 2 year cycle, doubling density every node

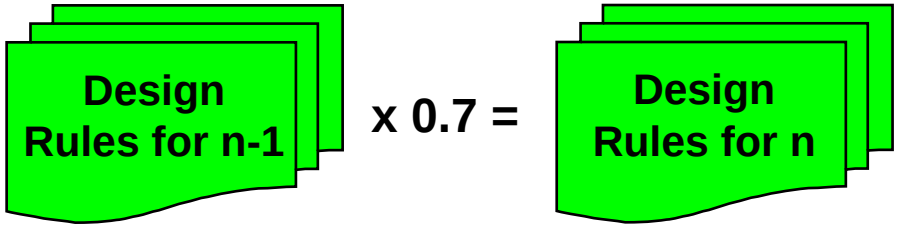
TMR = Technology Manufacturing Readiness

blue = DfM opportunities

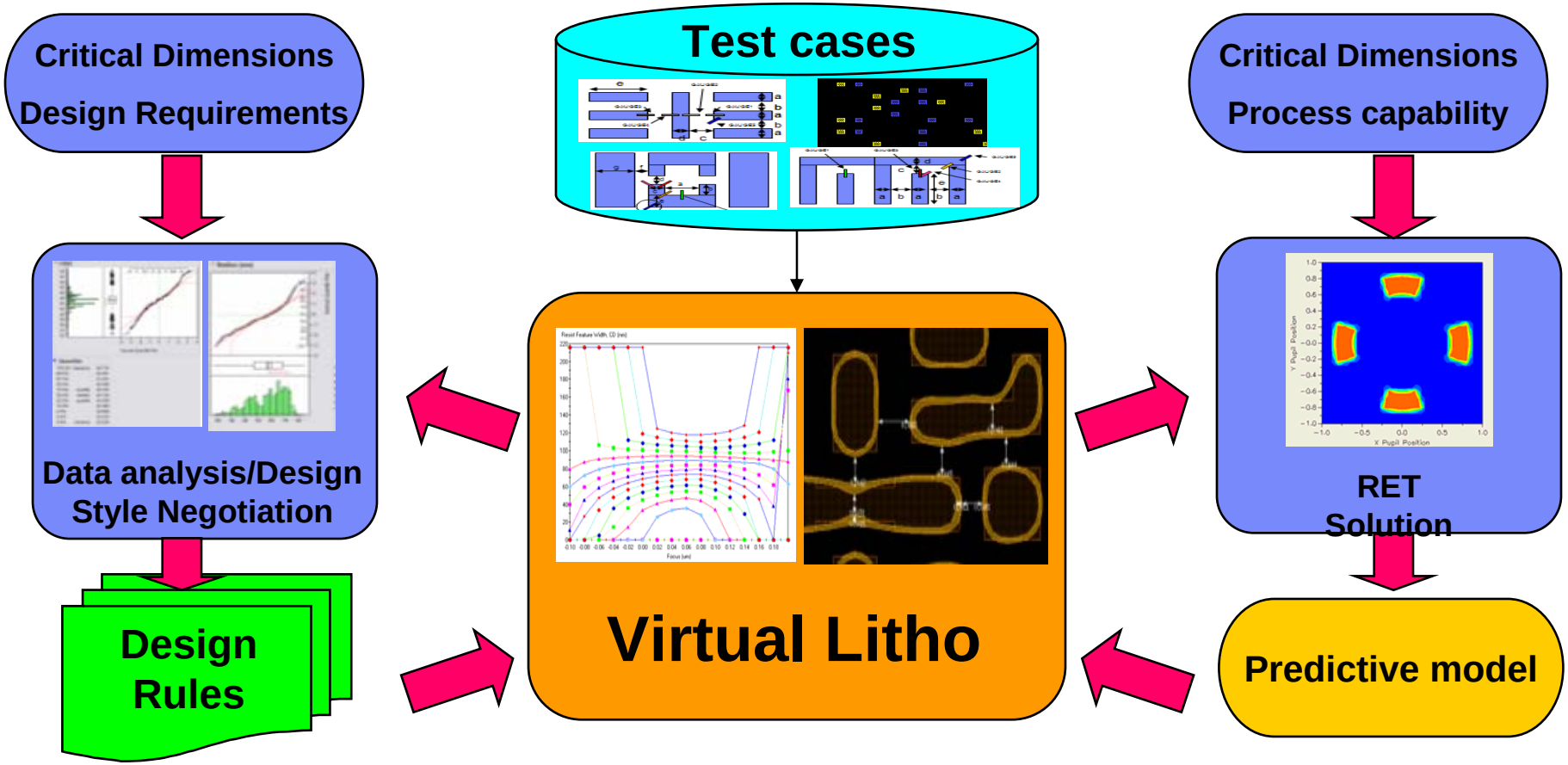
DfM in design rule optimization

T-2 — T-1 — T+

conventional design rule development (pre DfM):

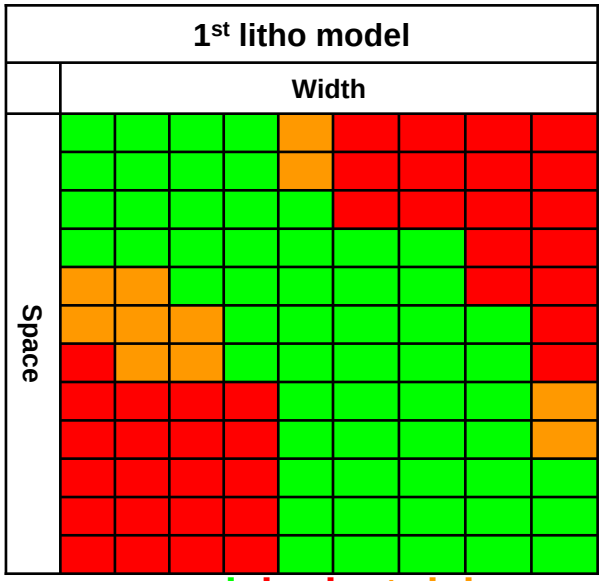


process-aware design rule development:

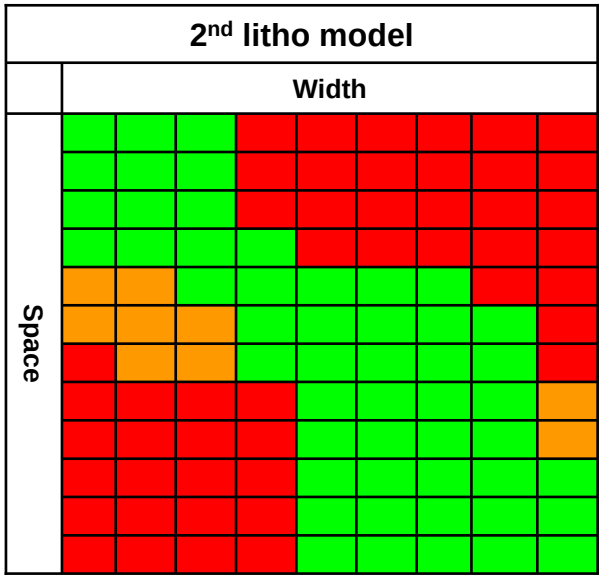


complex rules … that change

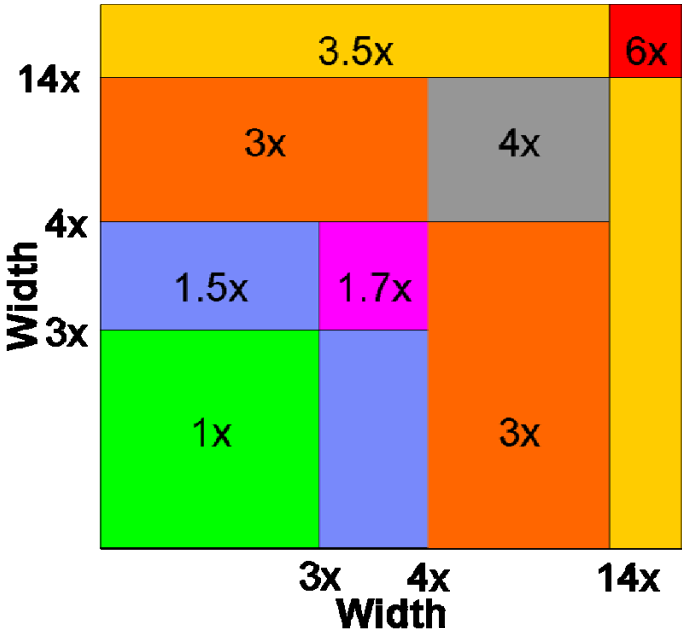
Metal Width Variability



good, bad, at risk



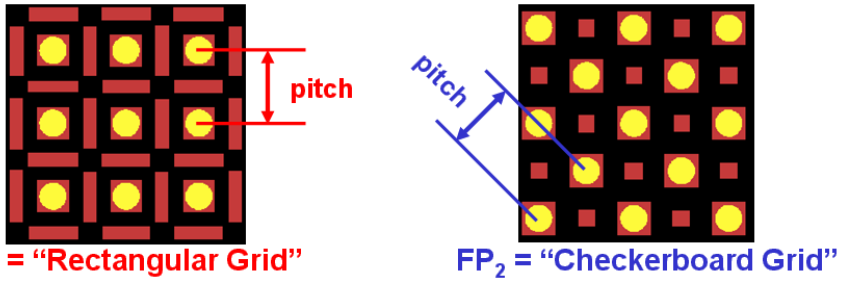
minimum space as a function of drawn width and neighboring width

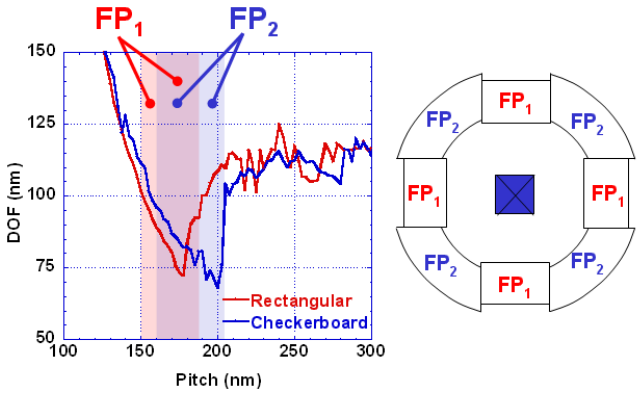


non-monotonic behavior of OAI + SRAF causes annoyingly complex design rules

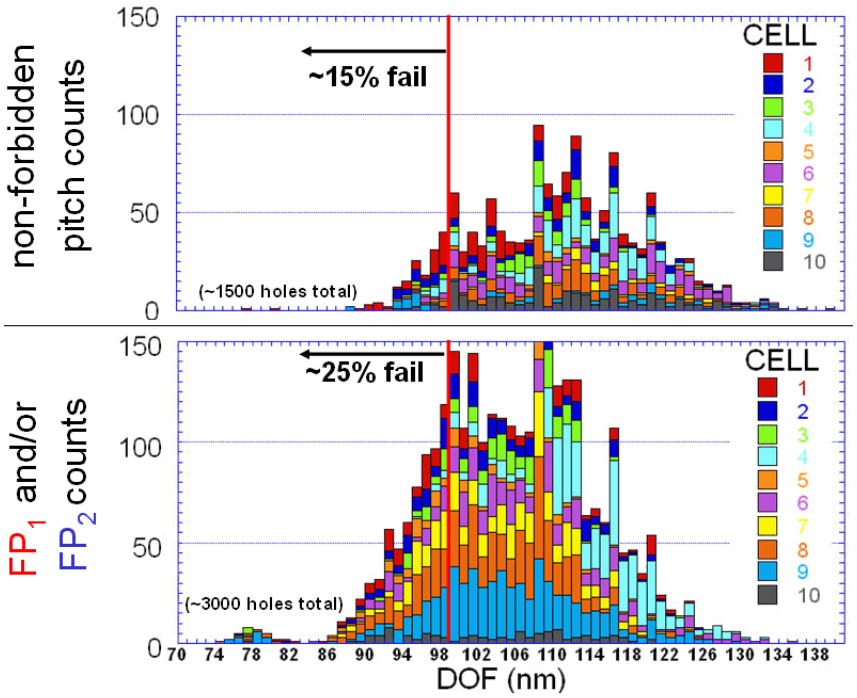
changes in the process (e.g. print bias due to etch optimization) and improvements in model accuracy make optimized design rules a moving target

Rule to enforce forbidden pitch in via layout





Correlation to Lithography Simulation

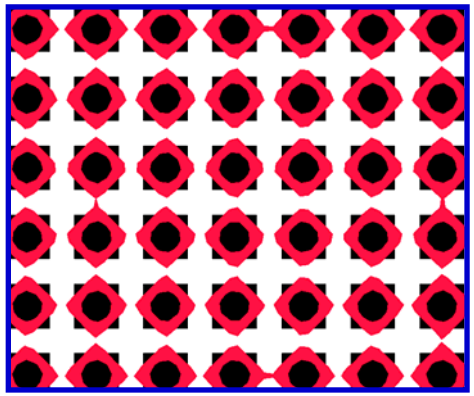


design flow challenges:

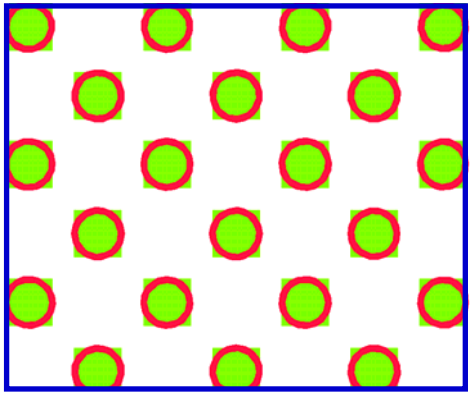
- **cell to cell interaction (post placement errors)**
- **via to pin interaction (post routing errors)**

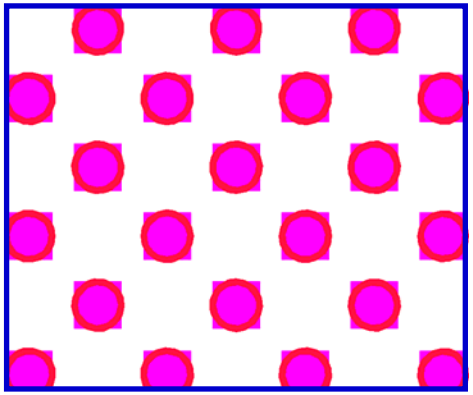
Inverse lithography as a DFM tool: accelerating design rule development with model-based assist feature placement, fast optical proximity correction and lithographic hotspot detection, Steve Prins, et al. Proc. SPIE 6925, 69250E (2008)

contact array at
k_1= .35

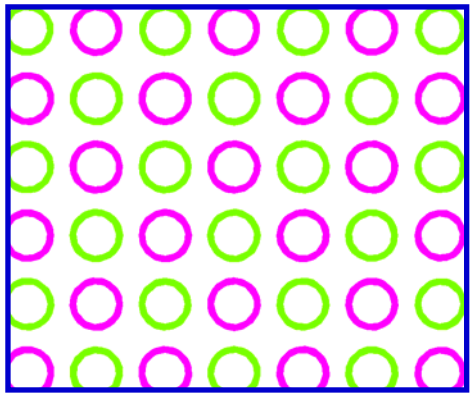


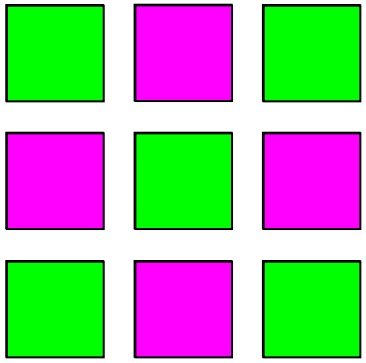
2 contact arrays at
k_1= .7



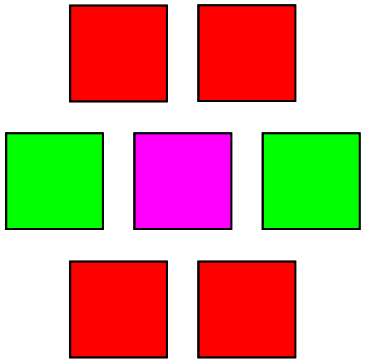


double patterning
with effective k_1= .35

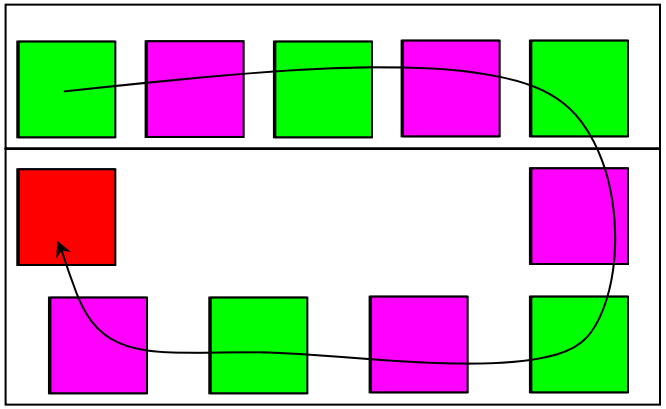




'T' error



'odd-even' error

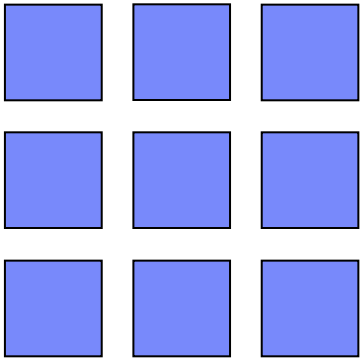


Layout topology conflicts are very similar to alternating PSM:

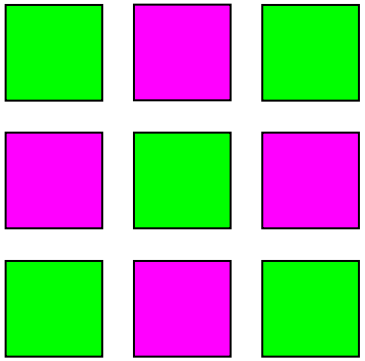
- **complex and non-local**
- **extend across cell boundaries**
- **impossible to capture with reasonably aggressive conventional rules**

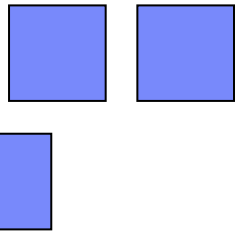
problem can cross cell-boundaries

conservative design rule:

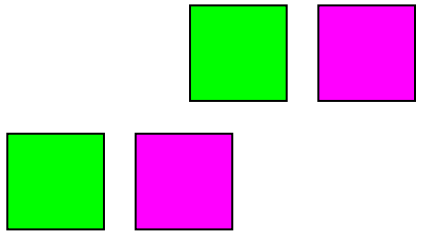


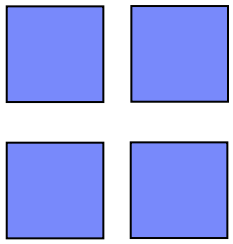
too many contacts at minimum space



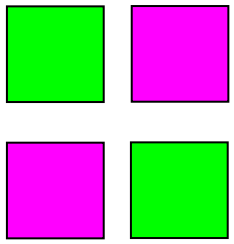


misaligned contact at minimum space





intermediate small space between contacts



Challenge:

- working with a partial set of partially accurate models
- process being modeled keeps changing
- rules have to be conservative enough to maintain a practical design flow
- rules have to be conservative enough to account for worst layout case

Not an option:

- freeze process earlier to build more accurate models for aggressive rules

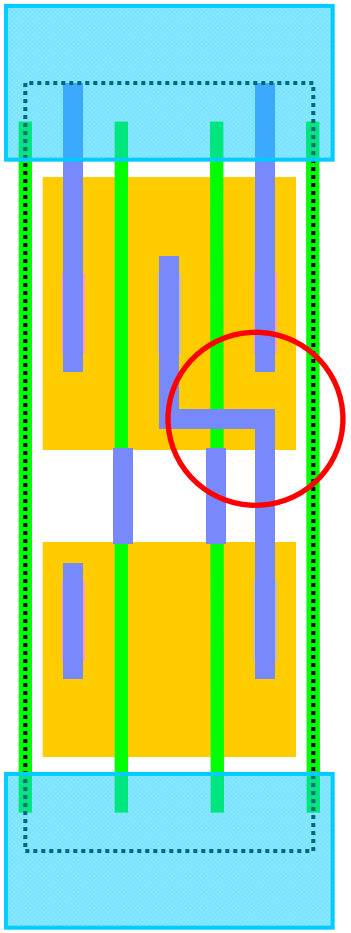
Possible options:

- coarse grid design rules enforce coarser design rule decisions
- maintain flexibility to adjust detailed rules as process becomes clearer

DfM in cell image definition

T-2 — T-1 — T+

strap power
with metal 1



Metal 2

Metal 1

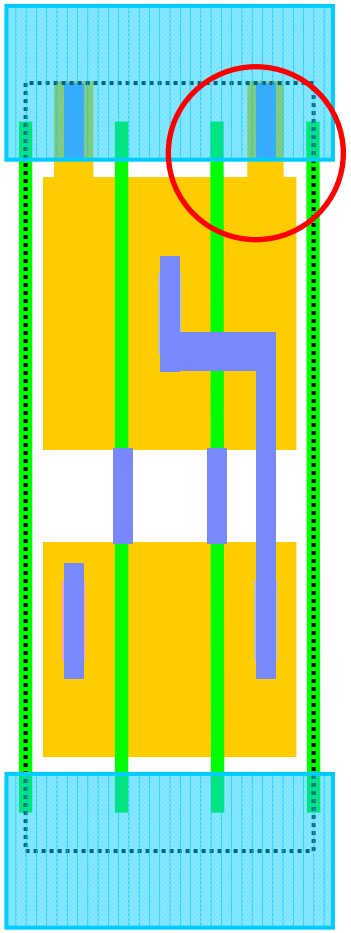
Poly

Diffusion

hotspot risk

routing congestion

strap power
with diffusion



gate width variation
(litho corner rounding)

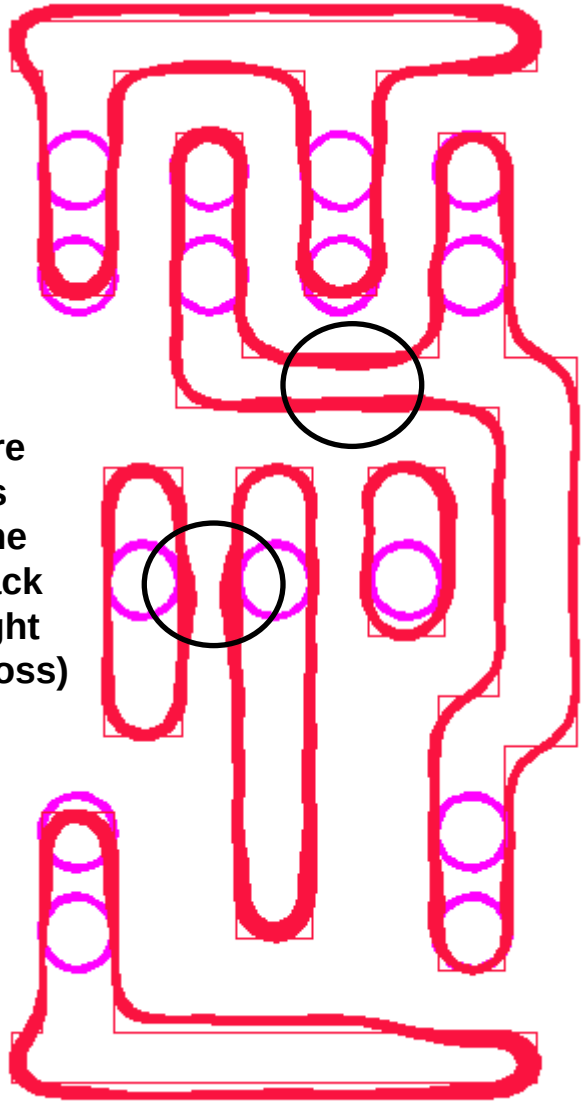
silicide resistance
variation

Even very fundamental topology decisions require accurate physical and electrical models

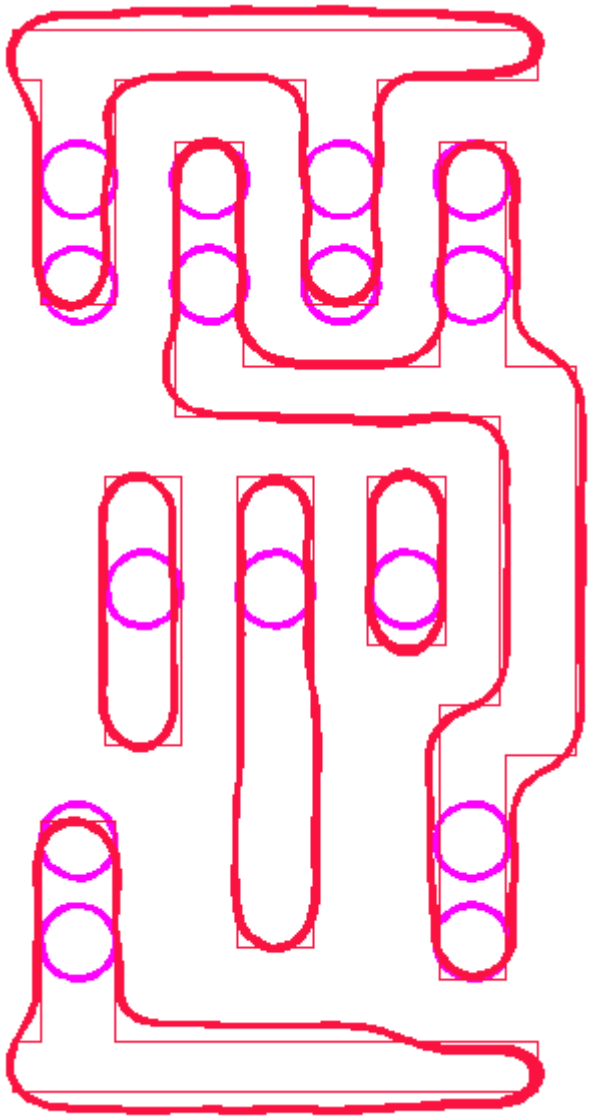
Outcome: compromised layout derived from in-depth engineering discussions

(or: follow 'customer is always right' principle and hope for the best)

2nd litho model



3nd litho model

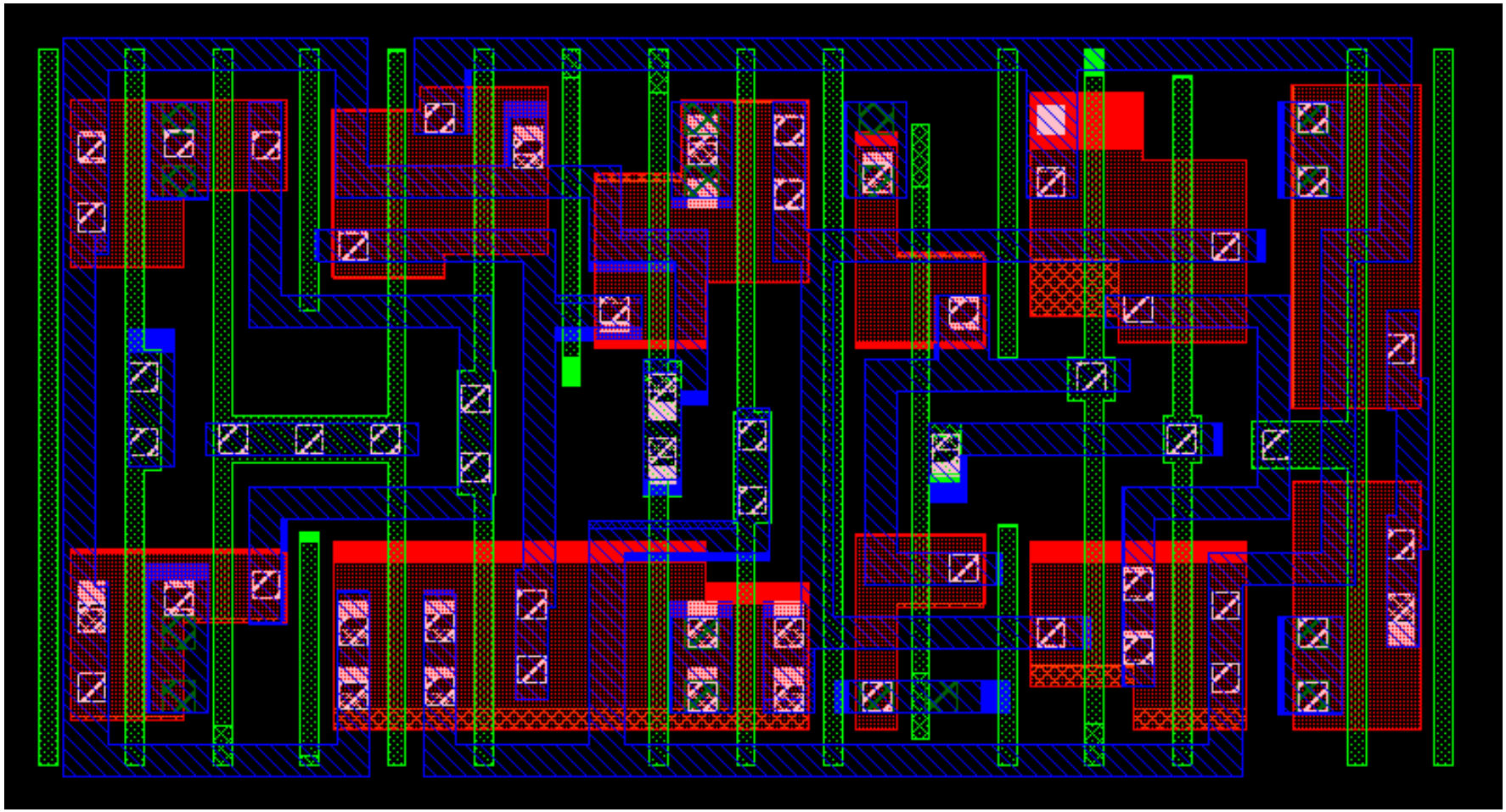


if these fails are real, designers have to add one more metal track to the cell height (10% density loss)

how will the answer change when etch modeling is added to the analysis?

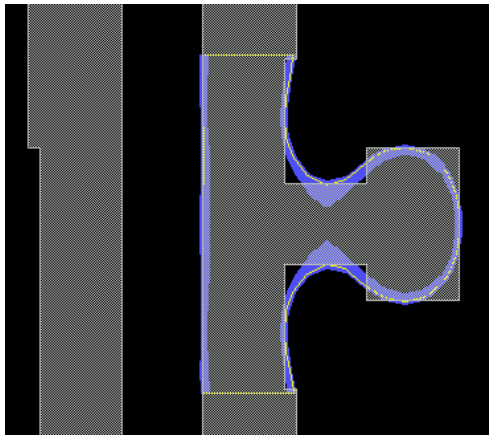
DfM in library optimization

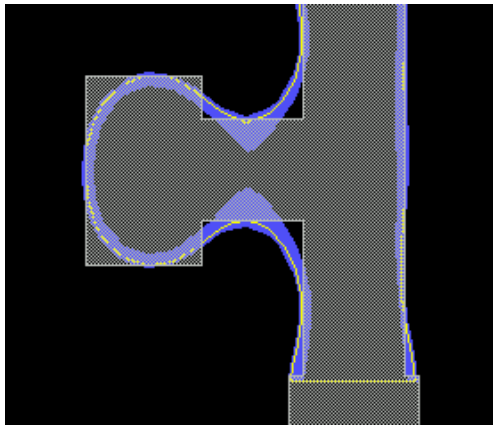
T-2 — T-1 — T+



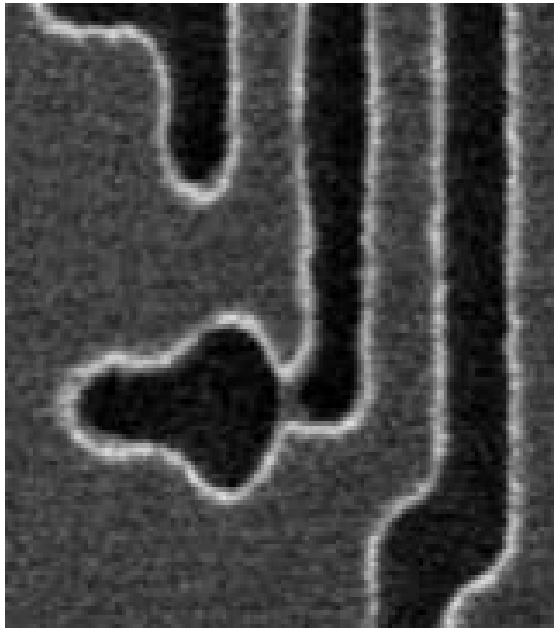
+ process maturing and stabilizing, litho models adequately accurate
+ automatic layout optimization tools demonstrated to work reliably
- litho models alone can not capture variety of yield risks as well as recommended rules
- characterization and quantification of r-rules carried over from previous node
- at this point layouts are largely finalized and leave little room for optimization

DfM in routing optimization



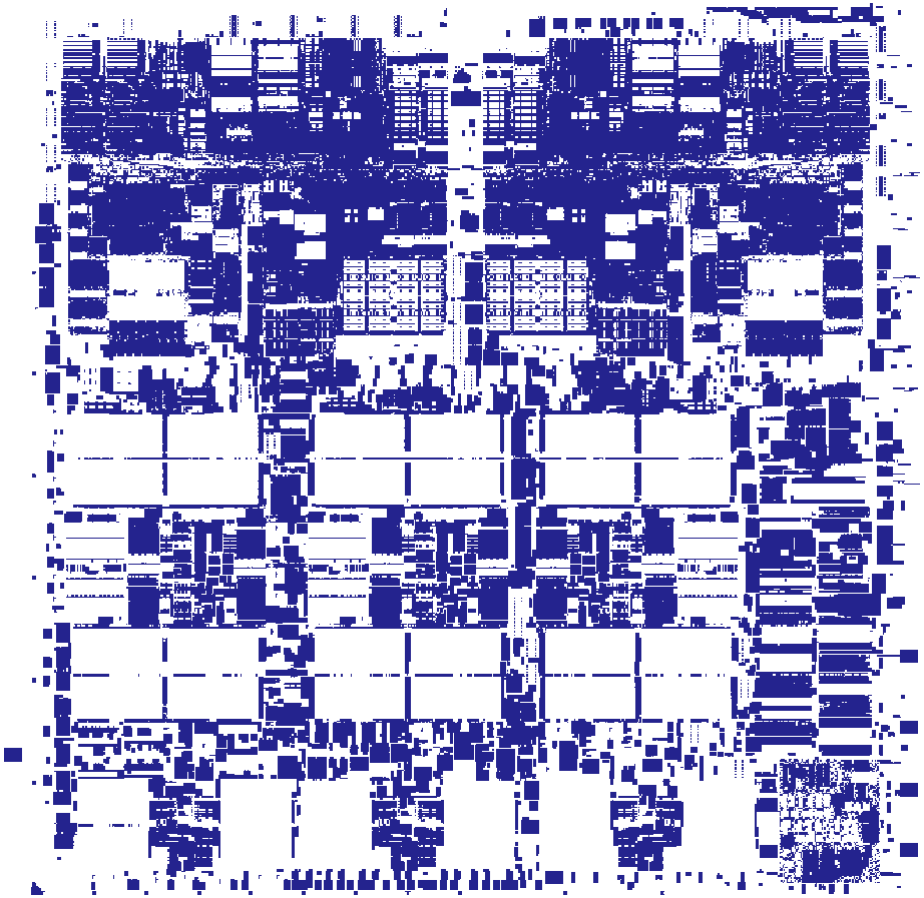


- router generated ‘hotspots’ do exist
- on rare occasion, they make it past the fab’s litho checks



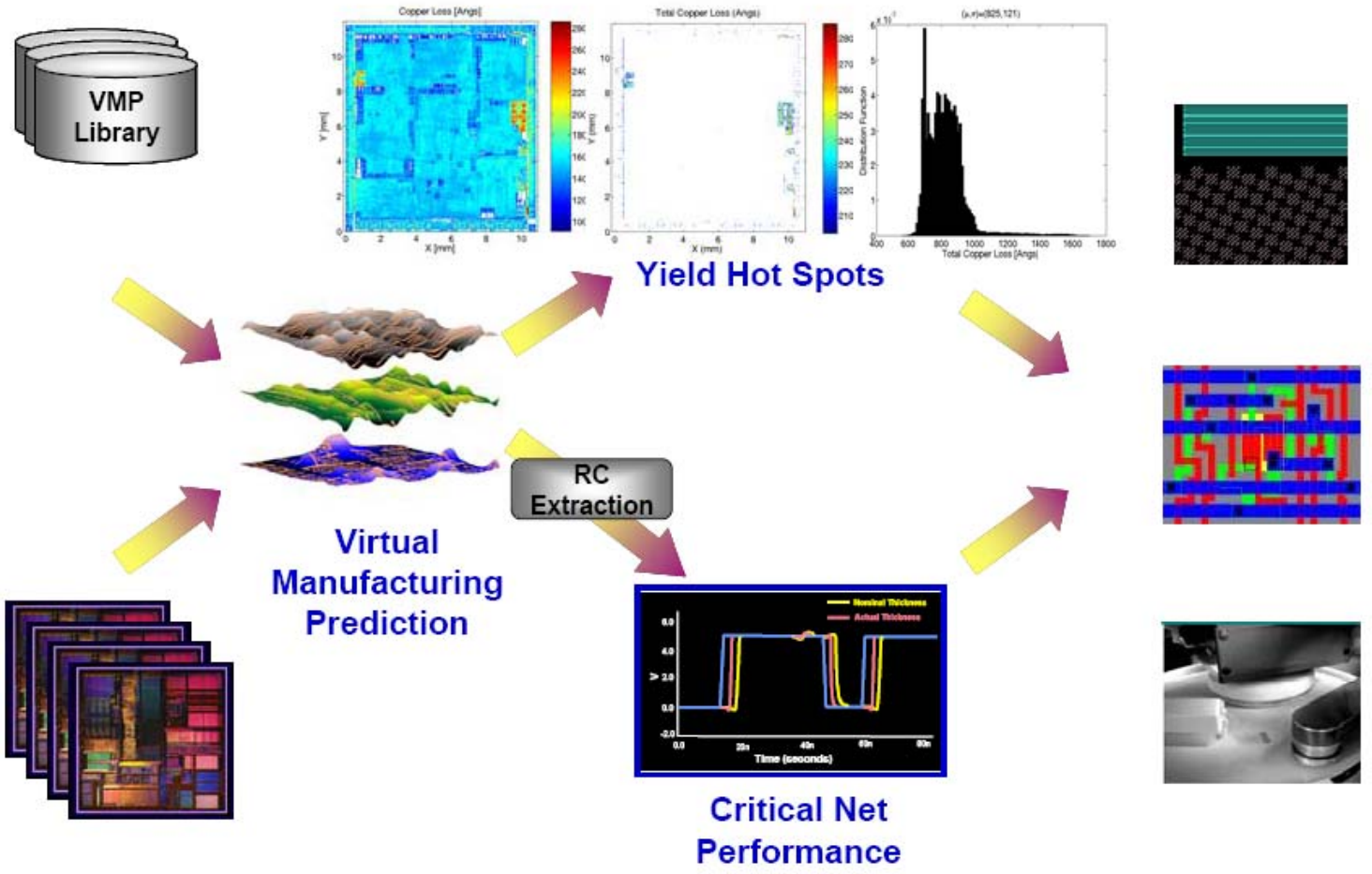
Full process-window modeling of full chips during routing is runtime prohibitive.
Speed-ups based on pre-filtering followed by local modeling proven functional.
Further development needed to reduce reliance on accurate ‘seeding’ of the filter.
Extension to other process phenomena and fail mechanisms remains a challenge.

post-routing redundant via insertion



<u>post place&route chip optimization:</u>

+ doesn't require changes in existing design tools (optimized for runtime, quality, ease-of-use)
+ can react to late changes in design and/or process



SPIE DfM'09: Hotspot Detection and Design Recommendation Using Silicon Calibrated CMP Model, Chartered Semiconductor Manufacturing Ltd, Singapore, IBM, NY, USA Freescale, Austin, TX, USA, Cadence Design Systems, San Jose, CA, USA

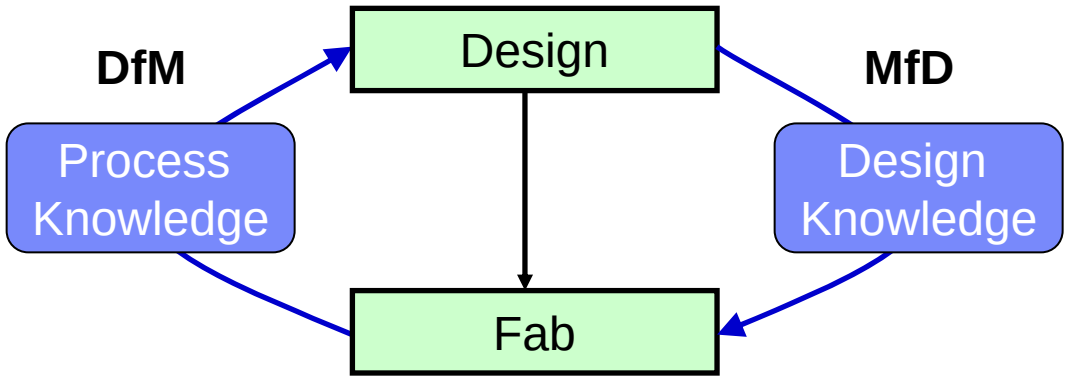
DfM value assessment

	Demonstrated Solution	Value Example
Cell/IP	a. automatic layout optimization for rules and models b. litho-aware extraction	a. 10% reduction in gate width variation b. identifies sensitivities
Place	a. CAA aware cell-swapping	a. complex CLY vs PLY tradeoffs
Route	a. rules-optimized routing/cleanup b. auto litho hotspot elimination	a. 2% yield increase in 130nm b. reduction in hotspots
Timing	a. fill-aware timing b. CMP-aware timing c. statistical static timing analysis d. spatial correlation timing	a. impact varies (a lot) b. 1% delay reduction c. 2% margin reduction 2% yield improvement d. 5% performance increase
post-Design	a. power/performance gate biasing	a. 20% leakage reduction (90nm)

AMD, ARM, Chartered, Freescale, IBM, Infineon, Samsung, Sony, Toshiba

Incremental yield improvements from DfM are very expensive to quantify.

SPIE's Design for Manufacturability through Design-Process Integration II, 6925-1



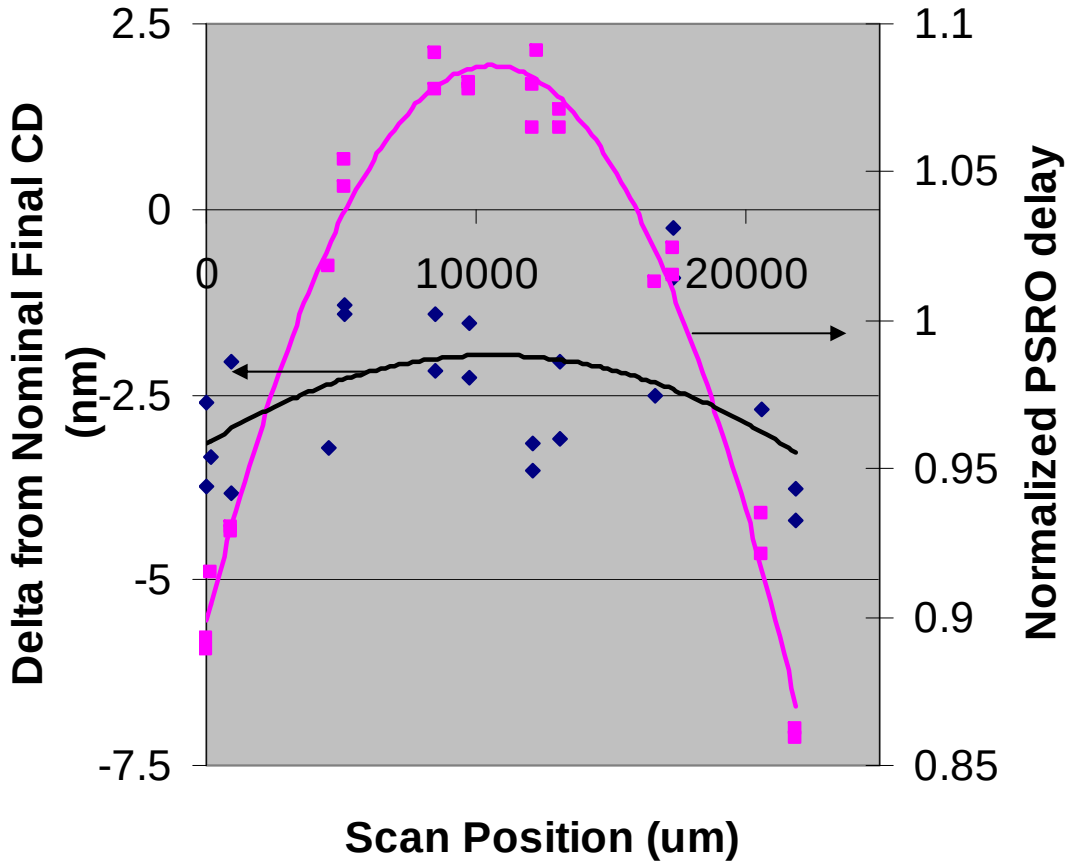
Examples of MfD:

- dose-mapper

- fill optimization for RTA

- electrically-driven OPC

MfD: Dosemapper



physical goal:
achieve dimensional uniformity

design intent:
minimize delay variation

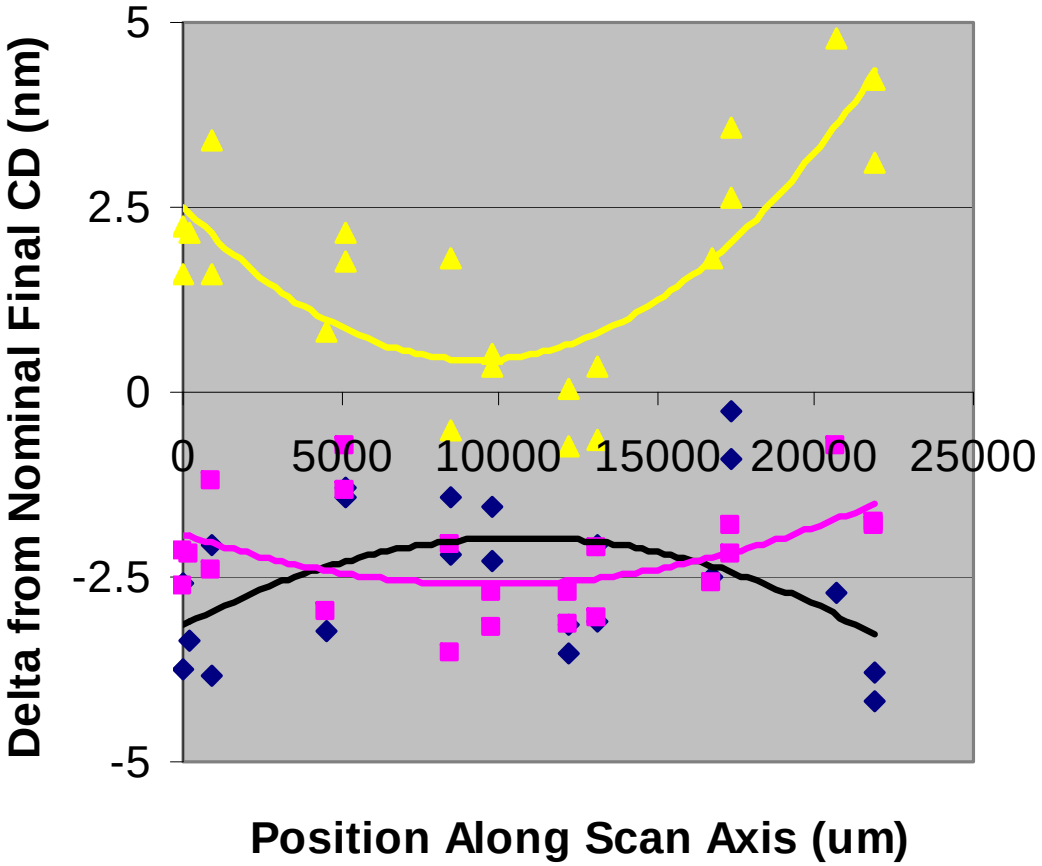
2nm etched poly-width variation → 21% delay variation

model predicts that 8nm width variation necessary to cause 21% electrical variation

Improving the power-performance of multicore processors through optimization of lithography and thermal processing, A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N Le, P. Lindo, A. P. Mahorowala, H-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas, and H. Utomo, Proc. SPIE 6521, 65210K (2007)

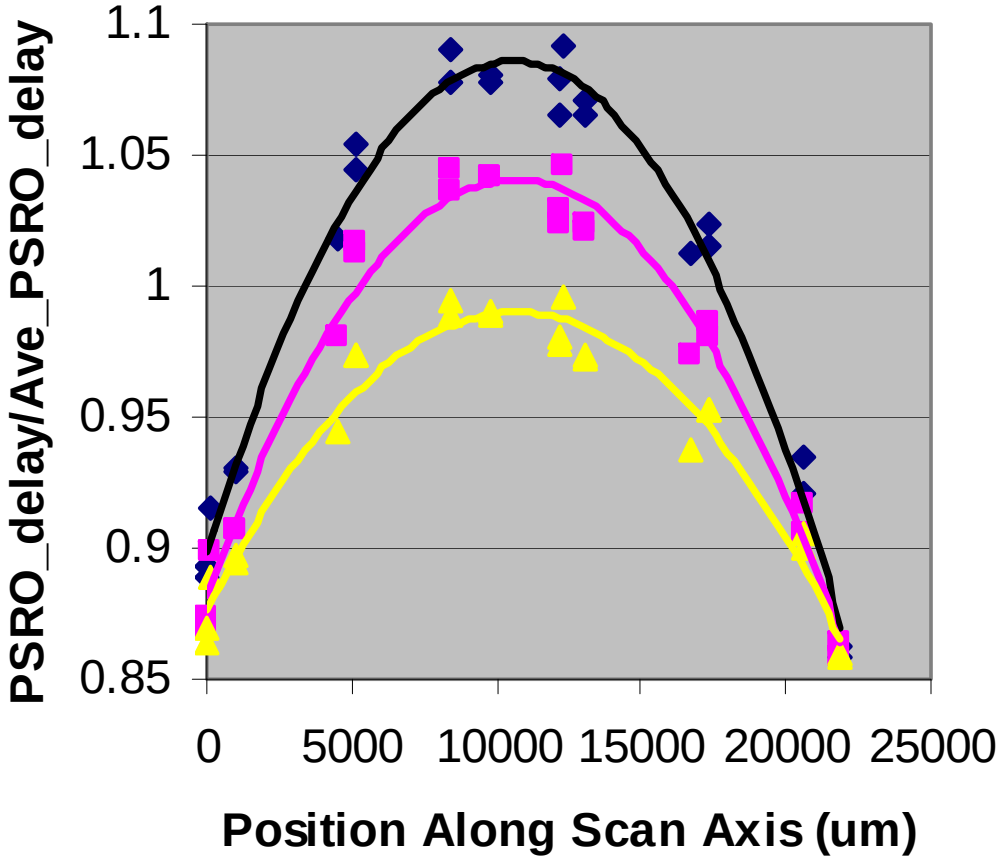
across field dose control

original (POR) - flat - smile
across field line-width distribution

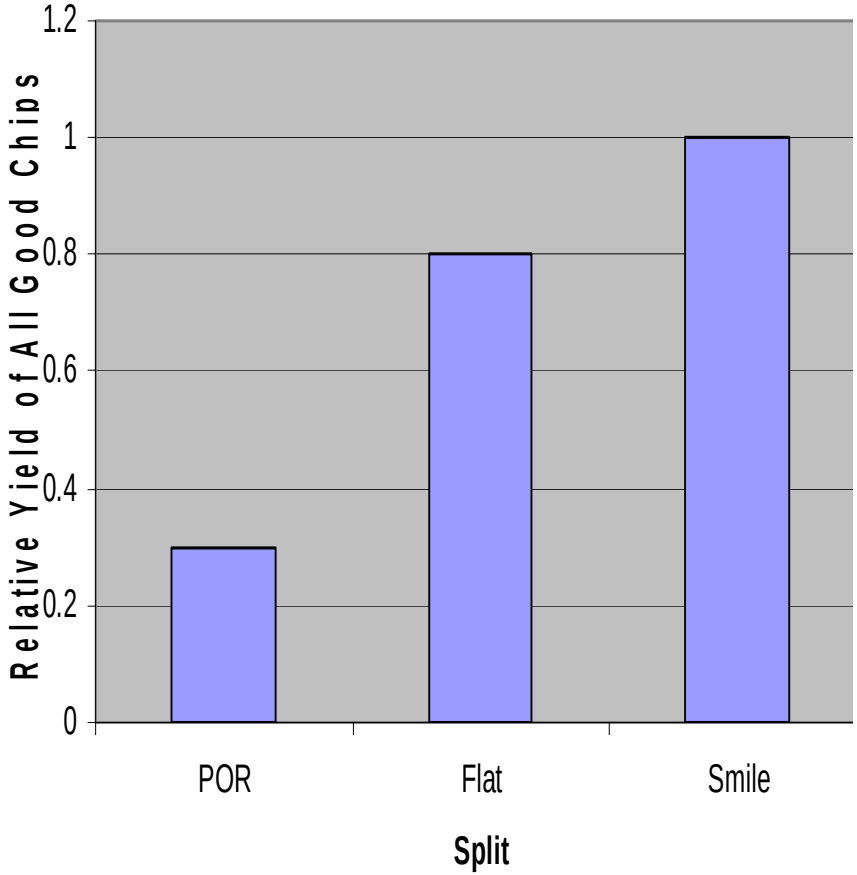


Improving the power-performance of multicore processors through optimization of lithography and thermal processing, A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N Le, P. Lindo, A. P. Mahorowala, H-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas, and H. Utomo, Proc. SPIE 6521, 65210K (2007)

original (POR) - flat - smile
across field delay distribution



yield improvement



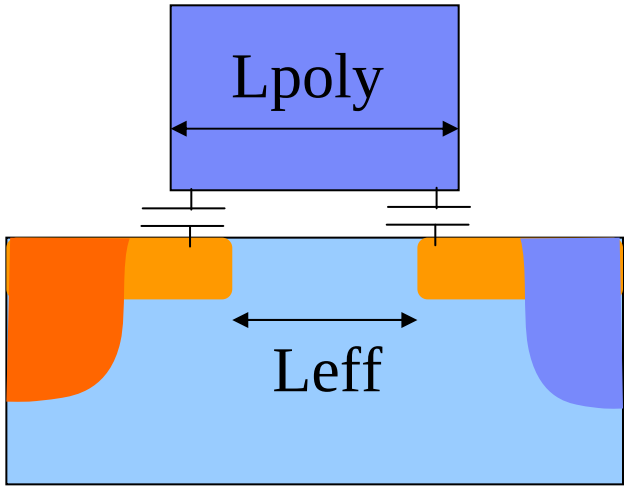
Improving the power-performance of multicore processors through optimization of lithography and thermal processing, A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N Le, P. Lindo, A. P. Mahorowala, H-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas, and H. Utomo, Proc. SPIE 6521, 65210K (2007)

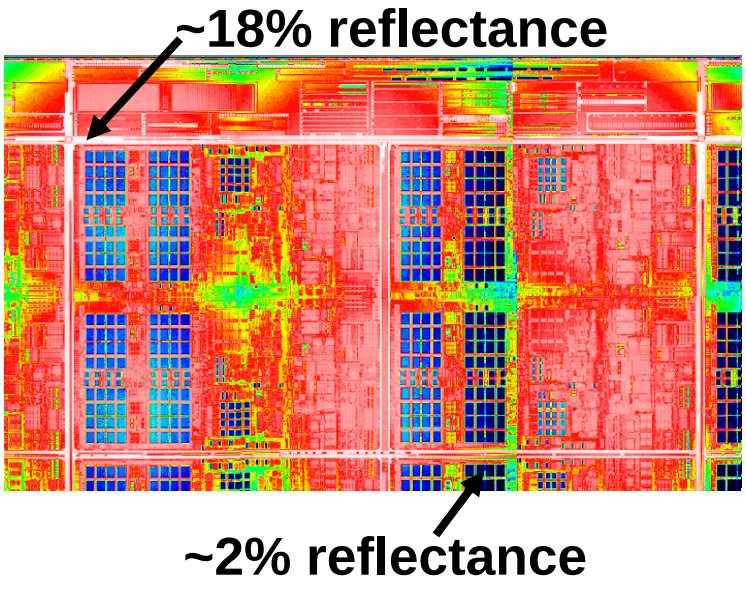
MfD: Rapid Thermal Anneal optimization

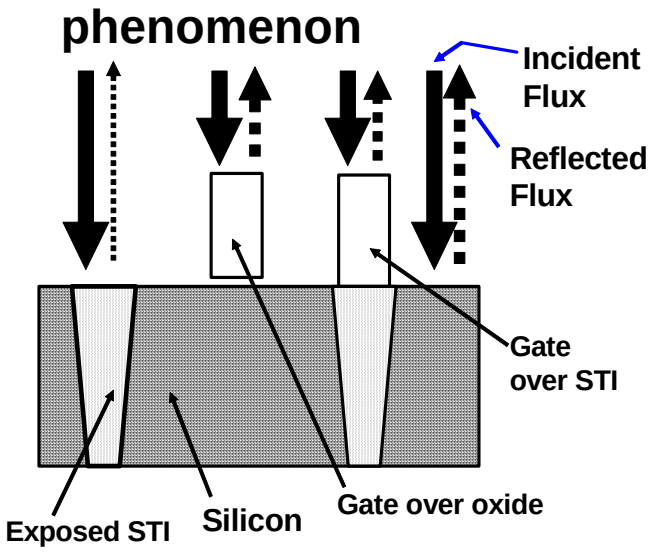
Rapid thermal anneal is used to drive dopants under the poly gate to reduce the effective channel length of the device.

A flash of infrared light is used to uniformly and quickly heat the wafer.

Reflectivity changes affect temperature uniformity.







MfD: Rapid Thermal Anneal optimization

% delay from each field's nominal delay

Original RTA process and fill

~25 mm across "scan"

-2.3%		-2.8%	
2.0%	4.1%	2.2%	0.9%
2.1%	4.4%	2.9%	0.7%
-3.6%	-2.4%	-3.7%	-4.6%

~25 mm across "slit"

max 4.4%

min -4.6%

Optimized RTA process and fill

~25 mm across "scan"

-0.8%		-0.7%	
0.0%	1.8%	-0.5%	-0.7%
0.0%	2.3%	1.0%	-0.8%
-0.9%	1.2%	-0.5%	-1.5%

~25 mm across "slit"

max 2.3%

min -1.5%

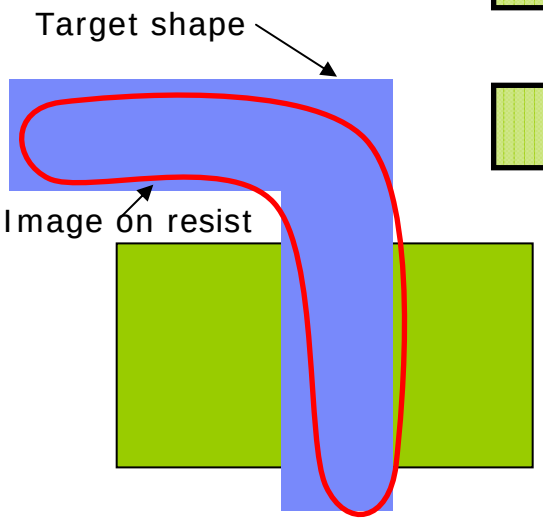
physical goal: achieve uniform pattern density on diffusion and poly

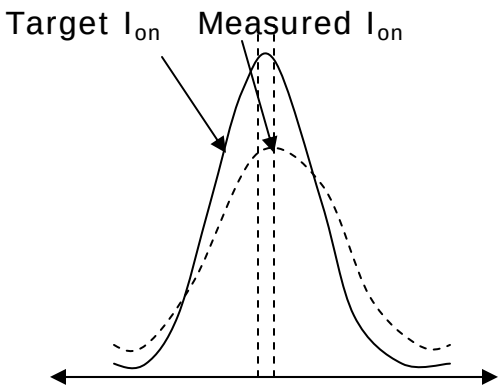
design intent: minimize delay variation

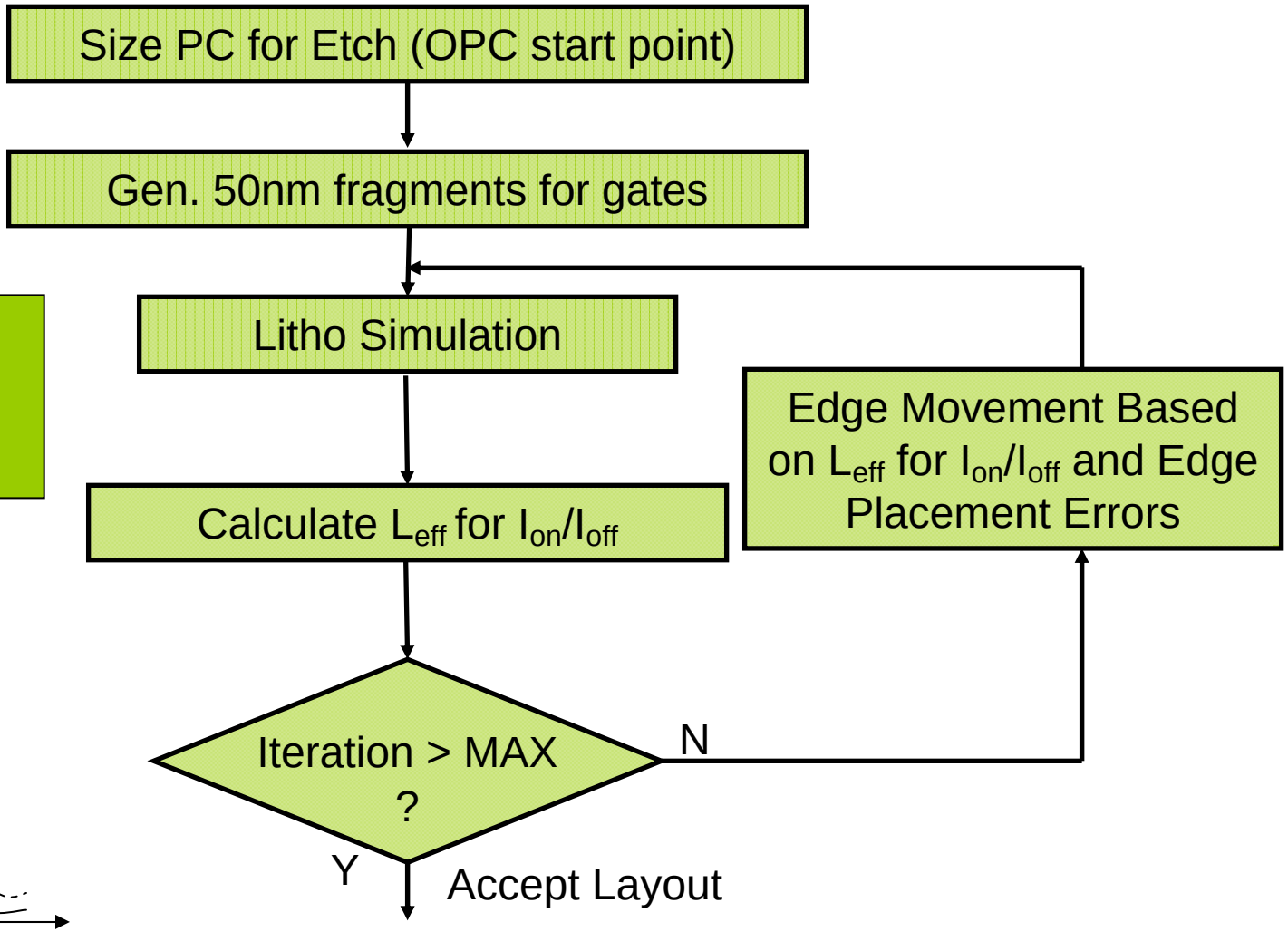
Improving the power-performance of multicore processors through optimization of lithography and thermal processing, A. H. Gabor, T. Brunner, S. Bukofsky, S. Butt, F. Clougherty, S. Deshpande, T. Faure, O. Gluschenkov, K. Greene, J. Johnson, N Le, P. Lindo, A. P. Mahorowala, H-J. Nam, D. Onsongo, D. Poindexter, J. Rankin, N. Rohrer, S. Stiffler, A. Thomas, and H. Utomo, Proc. SPIE 6521, 65210K (2007)

MfD: electrical OPC

5% improvement in timing accuracy over conventional OPC algorithms
50% reduction in the number of mask vertices on gate regions







Electrically driven optical proximity correction, Shayak Banerjee, Praveen Elakkumanan, Lars W. Liebmann, James A. Culp, and Michael Orshansky, Proc. SPIE 6925

MfD: challenges

Advantage of MfD (vs DfM)

- **feeds information forward in time!**
- **preserves the fab's need to tweak the process (some MfD may be a patch)**
- **centralizes the computational resources**

Challenges with MfD

- **correctly inferring 'design intent'**
- **preserving/improving CLY while improving PLY**
- **risk of introducing yield issues with data-prep challenges**

Outlook for future nodes

drive for more synergistic optimization of DfM and MfD

DfM – MfD Challenges

Incomplete set of process models.

Empirical models lack predictability.

Even for accurate process models (i.e. litho), failures are poorly modeled.

Can only feed information (design or process) forward in time.

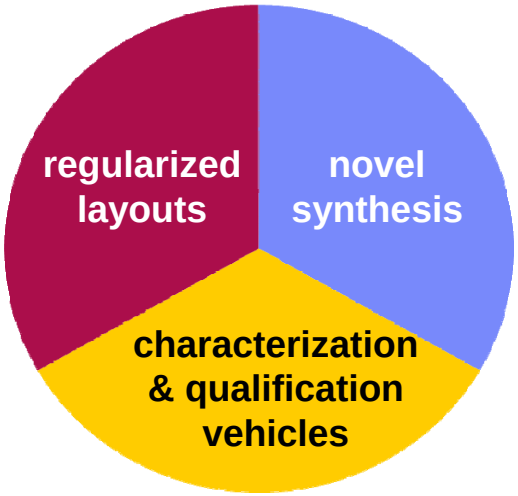
Can only react to information at hand (e.g. pre-placement cell optimization).

Can not enforce electrical accuracy by insisting on physical accuracy.

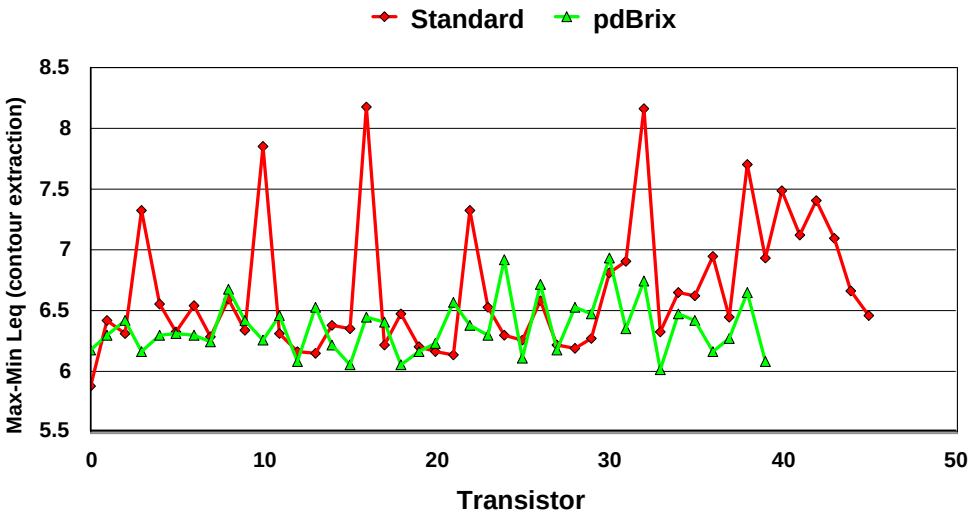
Full system-level design-process co-optimization will require leaps in computational efficiency.

Tactical Solution: RDR

pdBrix value proposition:

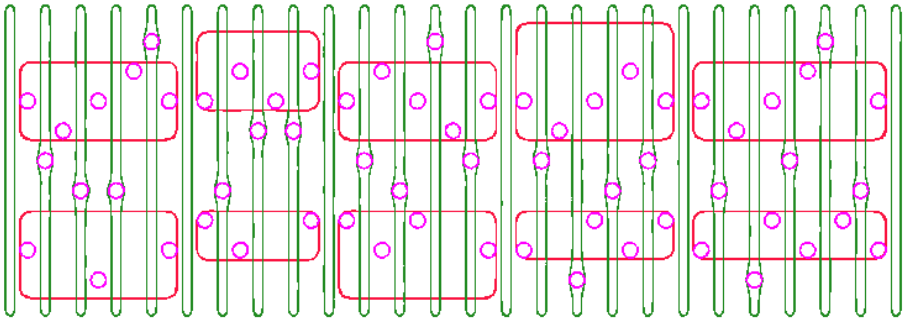


contour-based extraction including: dose, focus, mask size, and OL variation

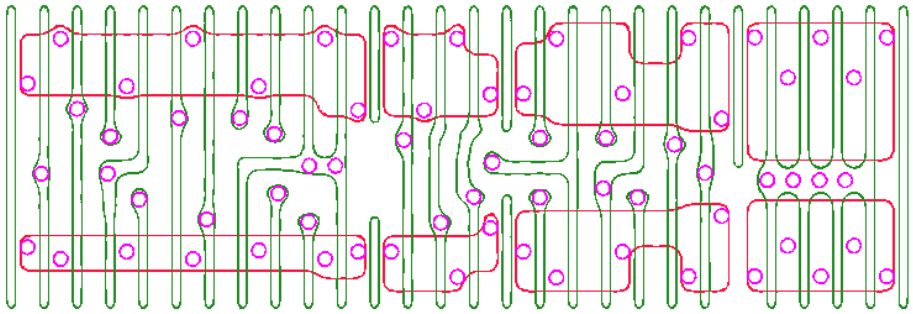


pdBrix design: sigma= 3.5nm
standard design: sigma= 4.1nm

pdBrix Cell



Standard Cell



SPIE DfM '09: Simplify to Survive, prescriptive layouts ensure profitable scaling to 32nm and beyond

Industry is in dire need of design-technology co-optimization.

Current DfM proposals fundamentally can't work.

Industry is in no position to invent revolutionary DfM.

If we continue to try to milk established solutions we will fail.

Industry-Academia collaborations are in the best position to seed innovation.

Discuss these views, brainstorm on potential solutions, do the research.

Benefit: there may still be a Semiconductor industry to graduate into.

Conclusion

DfM Dichotomy

Early in the process-technology development cycle:

processes are unstable, empirical models (and r-rules) are inaccurate, new layout sensitivities are unknown

Late in the process-technology development cycle:

layout optimization is constrained by the need to preserve timing, full-chip correction is constrained by computational resources

Tactical Solutions:

- **rely on the close collaboration between design, process, and device engineers**
- **expand the use of 'design-aware manufacturing'**
- **enforce highly regularized layouts that allow comprehensive process optimization**

Research Opportunity:

- **broader set of computationally efficient predictive process models**
- **design flows that allow dynamic physical-electrical co-optimization**